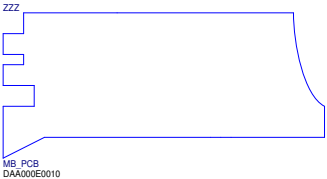


MODEL NAME : CAZ70  
PCB NO : LA-F051P  
BOM P/N : DAA000E0010



# Dell/Compal Confidential

## Schematic Document

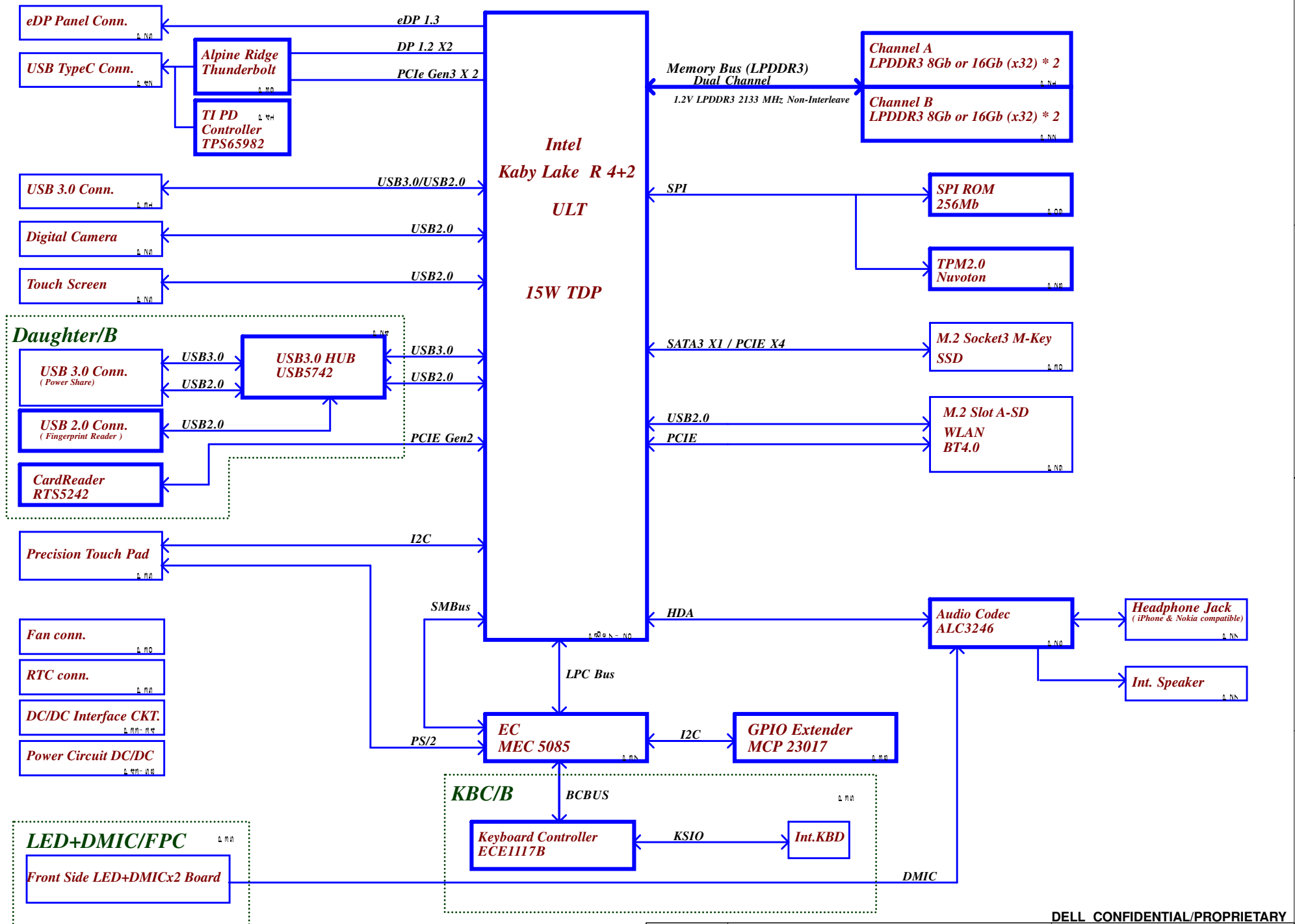
### Dino-R (Kaby Lake ULT)

2017-09-21

Rev: 1.0 (A00)

CPN	R1	R3	R3	R3
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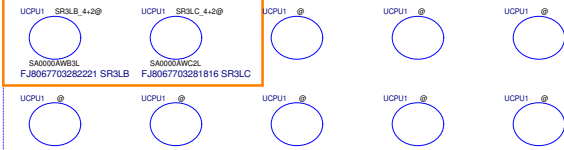
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#### 4+2 CPU Option PVT 007



#### AR Option



#### DRAM Option

#### DRAM Config Option

	UD19 MAG 1866@	UD20 MAG 1866@	UD21 MAG 1866@	UD22 MAG 1866@		MEM_CONFIG0 RH144 MAG 1866@	MEM_CONFIG1 RH139 MAG 1866@	MEM_CONFIG2 RH145 MAG 1866@	MEM_CONFIG3 RH151 MAG 1866@	MEM_CONFIG4 RH147 MAG 1866@
Micron 4G/1866	 SA0009XU1L D3 MT52L256M32D1PF-107WT.B PVT 010 SA0009XU1L SA0009XU1L SA0009XU1L SA0009XU1L					 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%
Micron 8G/1866	 SA0009U71L D3 MT52L512M32D2PF-107WT.B PVT 010 SA0009U71L SA0009U71L SA0009U71L SA0009U71L					 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%
Hynix 4G/1866	 SA0009G4L H3CCNNNBGTALAR-NUD SA0009G4L SA0009G4L SA0009G4L SA0009G4L				PVT 010	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Hynix 8G/1866	 SA0009F4L H3CCNNNBGTALAR-NUD SA0009F4L SA0009F4L SA0009F4L SA0009F4L					 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 4G/1866	 SA0009XY1L K4EBE324EB-EGCF SA0009XY1L SA0009XY1L SA0009XY1L SA0009XY1L				PVT 015	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 8G/1866	 SA0009CV1L K4EBE324EB-EGCF A31! SA0009CV1L SA0009CV1L SA0009CV1L SA0009CV1L					 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Hynix old die 8G/1866	 SA0009FJ1L H3CCNNNBGTALAR-NUD SA0009FJ1L SA0009FJ1L SA0009FJ1L SA0009FJ1L				PVT 014	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 16G/2133	 SA0009VY1L K4EBE324EB-EGCF A31! SA0009VY1L SA0009VY1L SA0009VY1L SA0009VY1L					 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Hynix 16G/2133	 SA0009ZL1L H3CCNNNBGTALAR-NVD SA0009ZL1L SA0009ZL1L SA0009ZL1L SA0009ZL1L					 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Micron 16G/2133	 SA0009ZV1L MT52L1G32D4PG-093WT.B SA0009ZV1L SA0009ZV1L SA0009ZV1L SA0009ZV1L					 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D

Board ID Table for AD channel

RE79	CE54	REV
4.3K	4700p	TBD
130K	4700p	TBD
62K	4700p	TBD
33K	4700p	TBD
8.2K	4700p	TBD
240K	4700p	A00
2.2K	4700p	X01
1K	4700p	X00

PVT 012

BOARD\_ID rise time is measured from 5% to 68%

SMBUS Control Table

	SOURCE	23017	BATTERY	Charger	PD	5085	XDP	Audio	Touch Pad
I2C1A_CLK I2C1A_DATA	MEC5085	V							
I2C1C_CLK I2C1C_DATA	MEC5085		V						
I2C1G_CLK I2C1G_DATA	MEC5085			V					
I2C2A_CLK I2C2A_DATA	MEC5085				V				
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH					V			
SMBCLK SMBDATA	PCH						V		
I2C0_CLK I2C0_DATA	PCH								
I2C1_CLK I2C1_DATA	PCH								V



CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Alpine Ridge
	CLKOUT_PCIE1	NGFF CARD WLAN	Lane 2	Alpine Ridge
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	M.2 SSD / PCIe	Lane 4	
	CLKOUT_PCIE4		Lane 5	NGFF CARD WLAN
	CLKOUT_PCIE5	Card Reader	Lane 6	Card Reader
	FLEX CLK#	DESTINATION	Lane 7	
	CLKOUT_LPC_0	EC LPC	Lane 8	
	CLKOUT_LPC_1	Debug	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

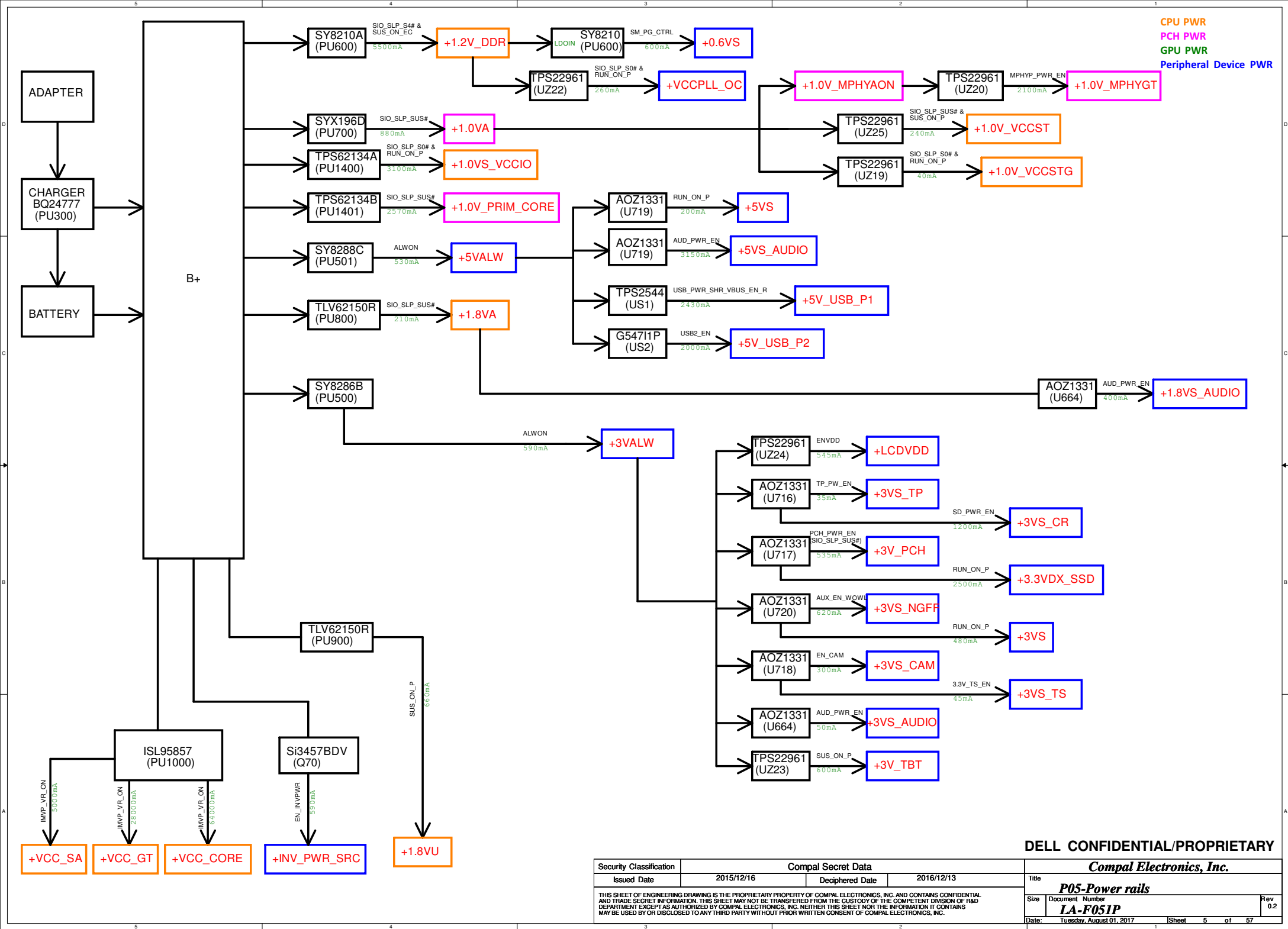
PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	External USB3(On IOB)
	2	External USB3(On MB)
	3	NGFF CARD WLAN
	4	Touch Panel
	5	Camera
	6	
	7	
PCH USB 3.0 Port Mapping	1	External USB3(On IOB)
	2	External USB3(On MB)

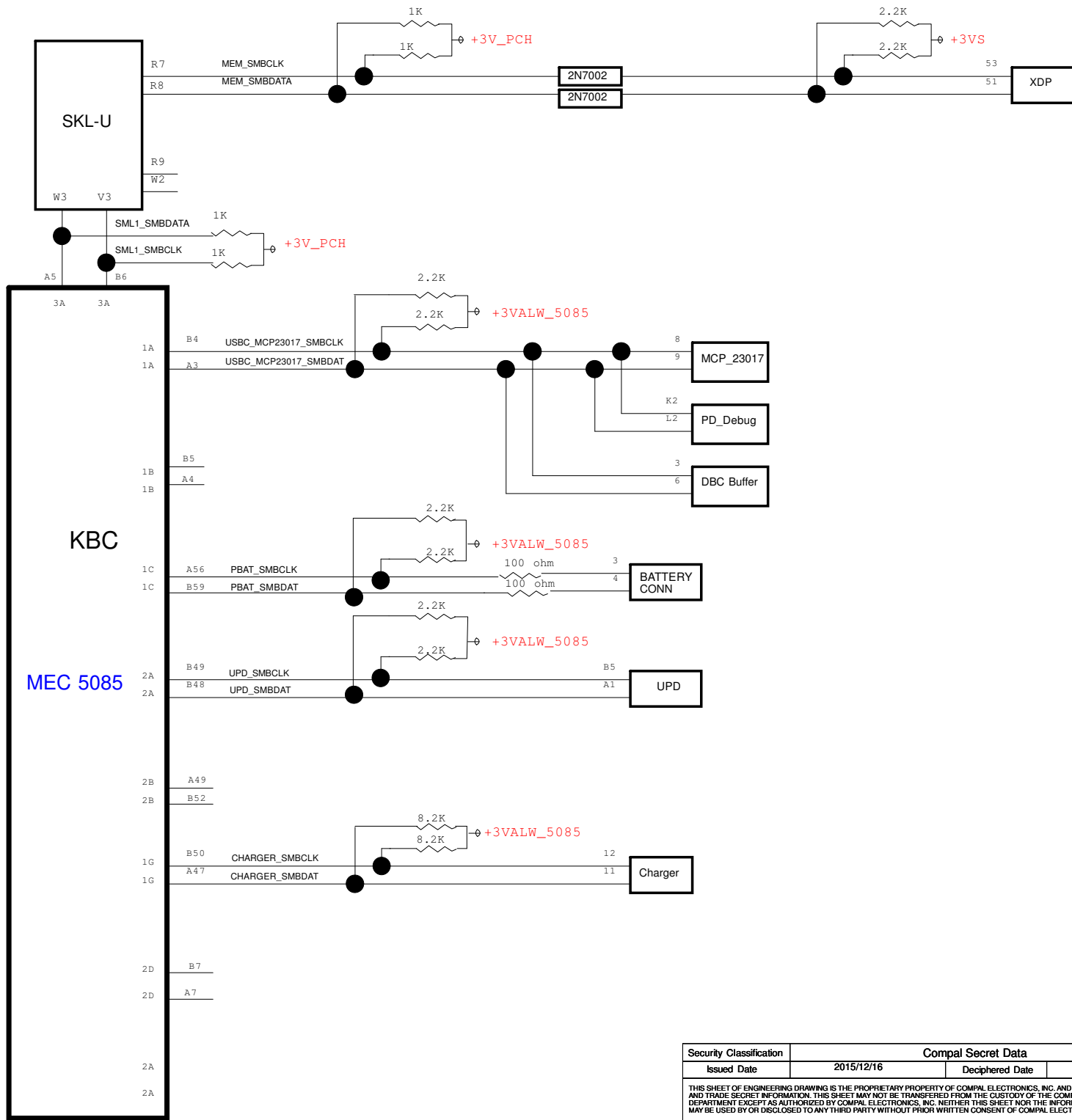
PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

SATA PORT#	DESTINATION
SATA-0	
SATA-1A	
SATA-1B	
SATA-2	M.2 SSD

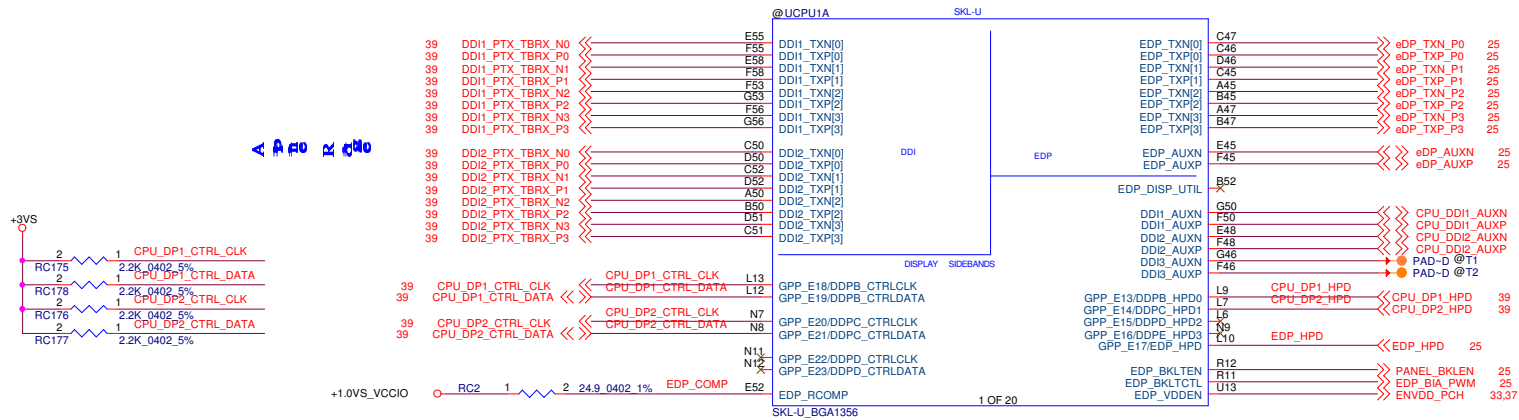
Symbol Note :

 : means Digital Ground  
 BOM symbol



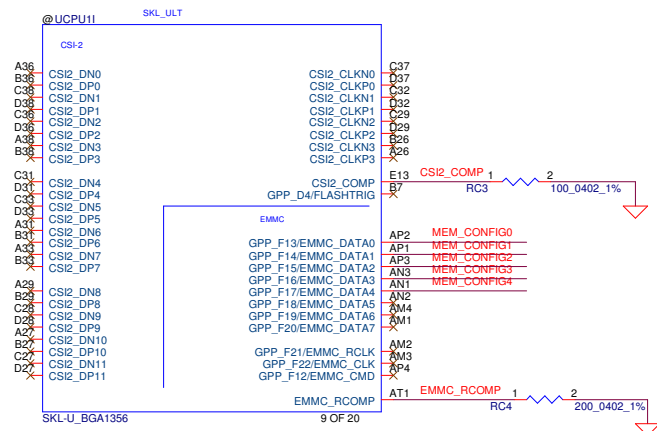


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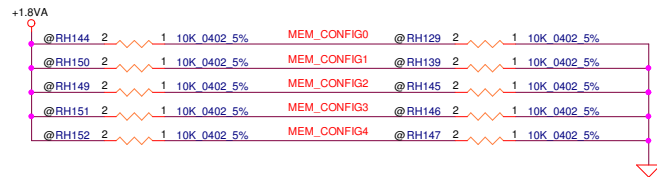


UCPU1A

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



DDR Memory Configurati no Type Strap ph



GPIO Pin	Pin Name		Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 1866/4G	Samsung 1866/8G	Samsung 1866/16G
GPP_F13	MEM_CONFIG0	1600 Mbps	0	1	0	1	0	1	0	1	0
GPP_F14	MEM_CONFIG1		0	0	1	1	0	0	1	1	0
GPP_F15	MEM_CONFIG2		0	0	0	0	1	1	1	1	0
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	0	0	1
GPP_F17	MEM_CONFIG4		0	0	0	0	0	0	0	0	0
GPIO Pin	Pin Name		Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	New Hynix 4G	New Hynix 8G	New Hynix 16G
GPP_F13	MEM_CONFIG0	1866 Mbps	1	0	1	0	1	0	1	0	1
GPP_F14	MEM_CONFIG1		0	1	1	0	0	1	1	0	0
GPP_F15	MEM_CONFIG2		0	0	0	1	1	1	1	0	0
GPP_F16	MEM_CONFIG3		1	1	1	1	1	1	1	0	0
GPP_F17	MEM_CONFIG4		0	0	0	0	0	0	0	1	1
GPIO Pin	Pin Name		Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_F13	MEM_CONFIG0	2133 Mbps	0	1	0	1	0	1	0	1	0
GPP_F14	MEM_CONFIG1		1	1	0	0	1	1	0	0	1
GPP_F15	MEM_CONFIG2		0	0	1	1	1	1	0	0	0
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	1	1	1
GPP_F17	MEM_CONFIG4		1	1	1	1	1	1	1	1	1

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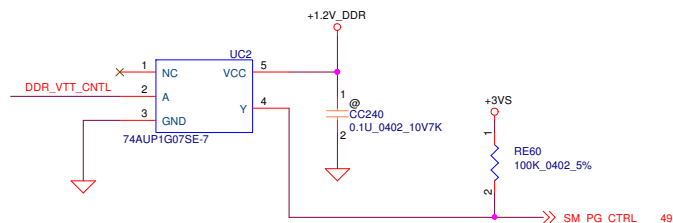
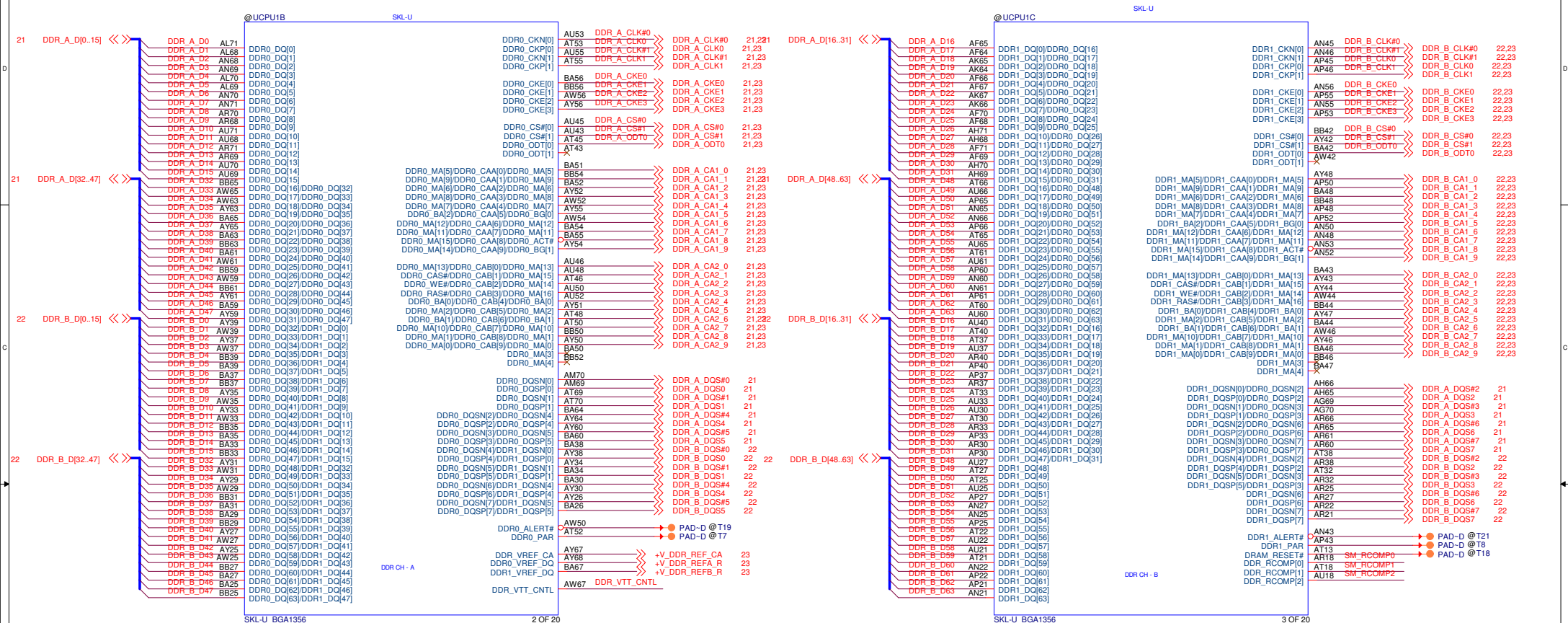
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Rev

0.2

### LPDDR3, Ballout for side by side(Non-Interleave)



**CAD Note:**  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

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SPI\_MOSI= SPI\_IO0  
SPI\_MISO= SPI\_IO1  
PCH EDS R0.7 p.235~236

+3V\_PCH

+3VS

+3V\_PCH

+3VS

+3V\_PCH

+3VS

+3V\_PCH

+3VALW

+3V\_PCH

+3VS

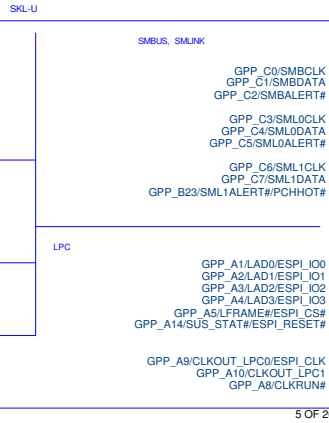
+3V\_PCH

+3VS

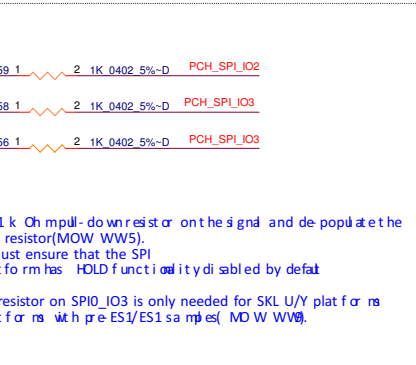
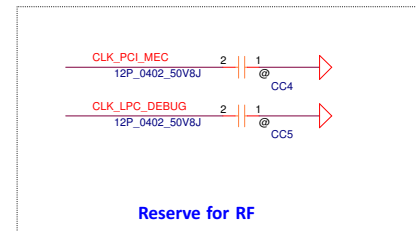
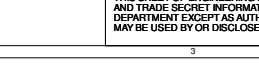
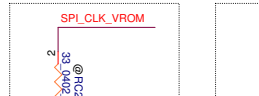
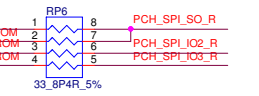
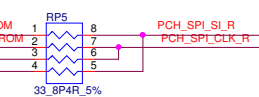
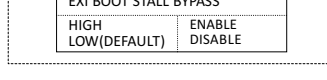
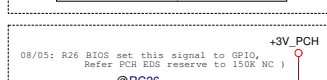
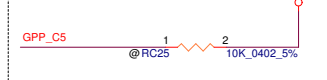
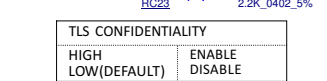
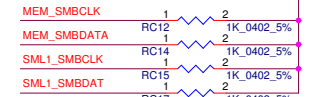
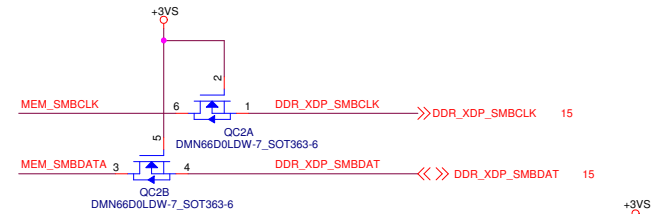
+3V\_PCH

+3VS

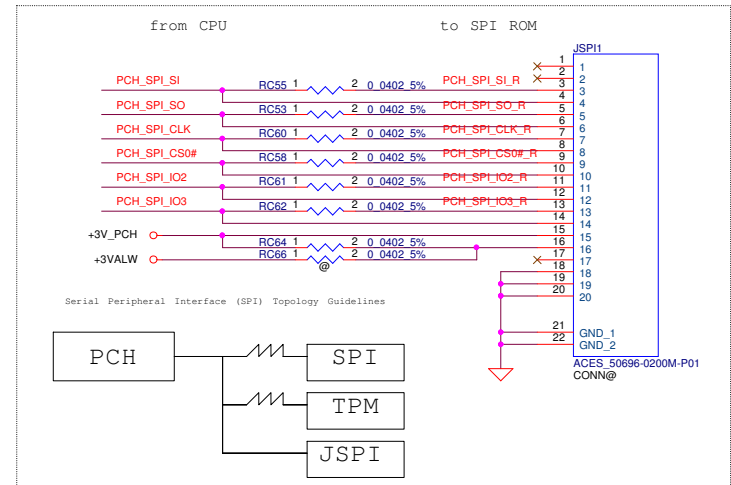
+3V\_PCH



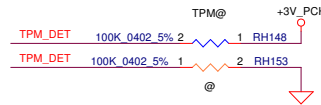
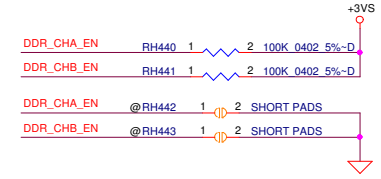
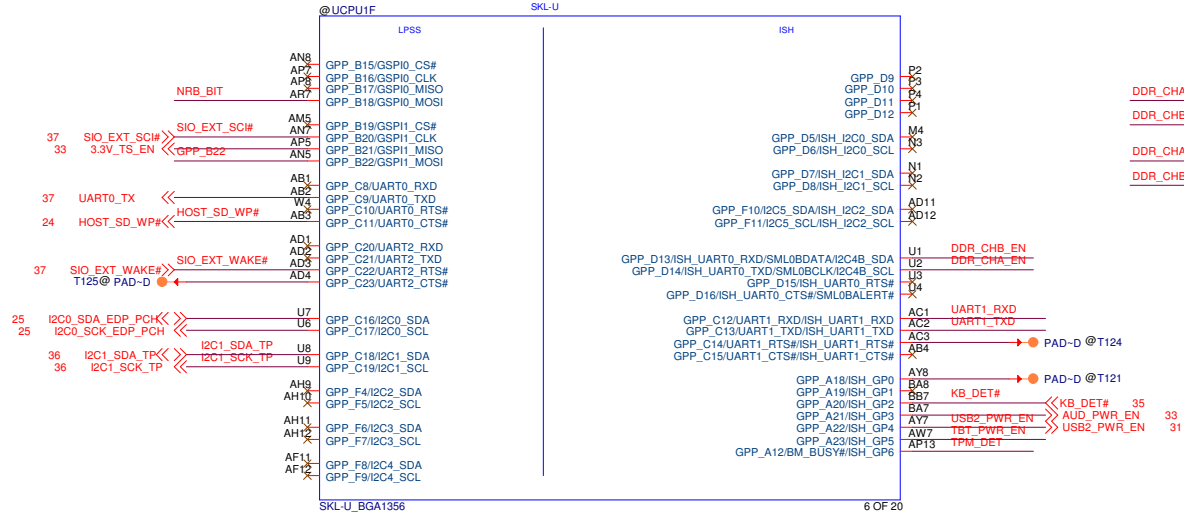
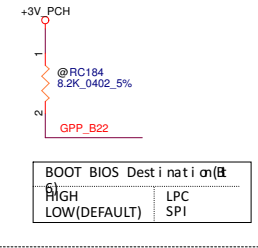
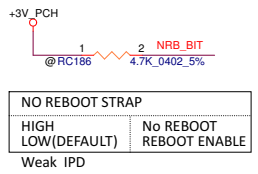
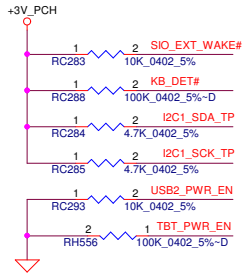
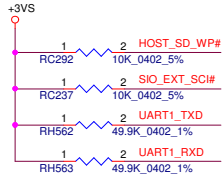
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9/5 MOW  
Option 1: Implement a 1k Ohm pull-down resistor on the signal and populate the required 1k Ohm pull-up resistor (MOW WW5).  
In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.  
Note that the pull down resistor on SPI0\_IO3 is only needed for SKL U/Y platform with ES and SKL S/H platform with ES1/ES1 sa mples (MOW WW5).

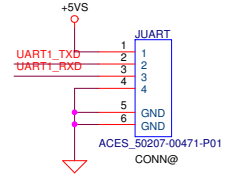


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				Document Number		
				LA-F051P		
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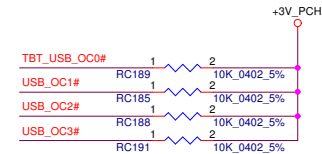
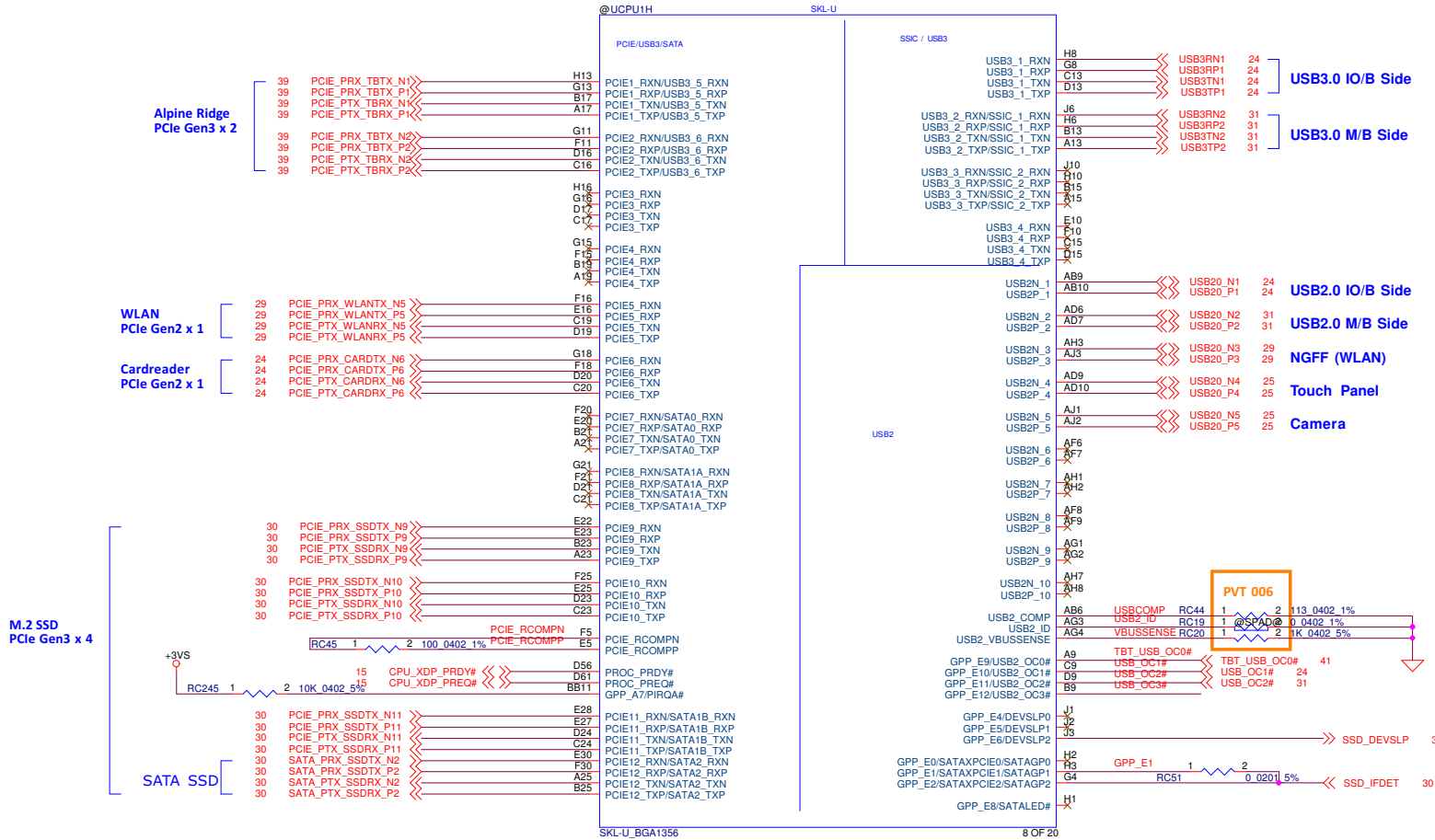
## TPM BOM Optional

TPM DET	
TPM	1 = W/TPM 0 = W/O TPM

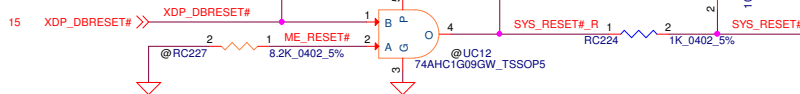
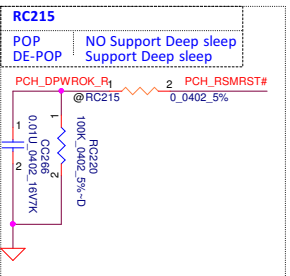
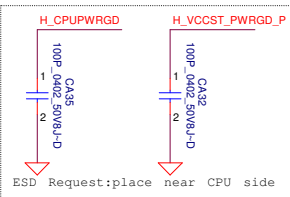
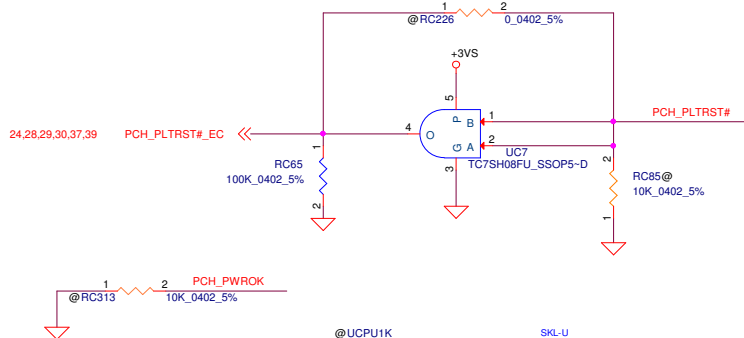
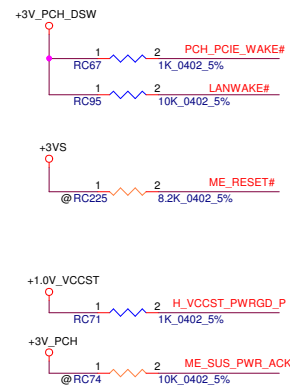
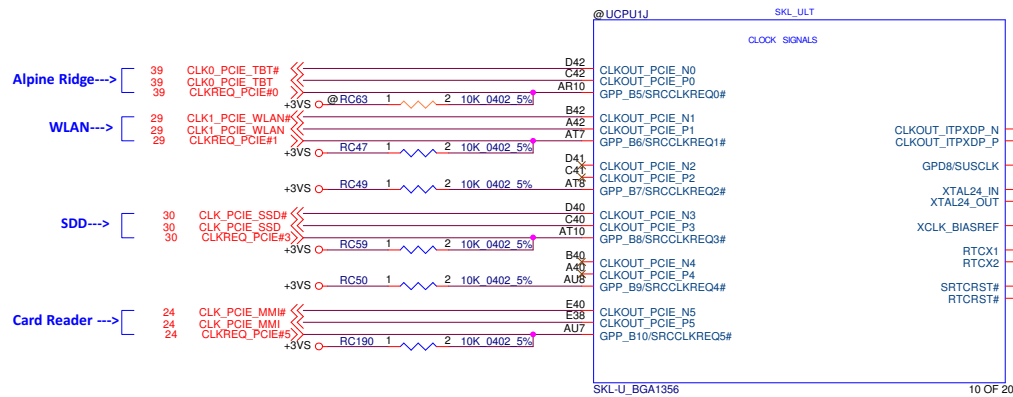


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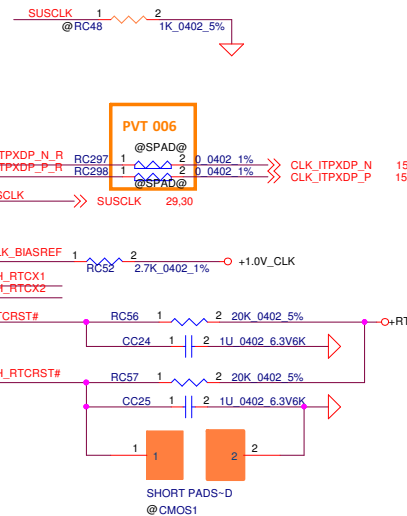
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Date: Tuesday, August 01, 2017	Sheet 10	of 57	Rev 0.2	



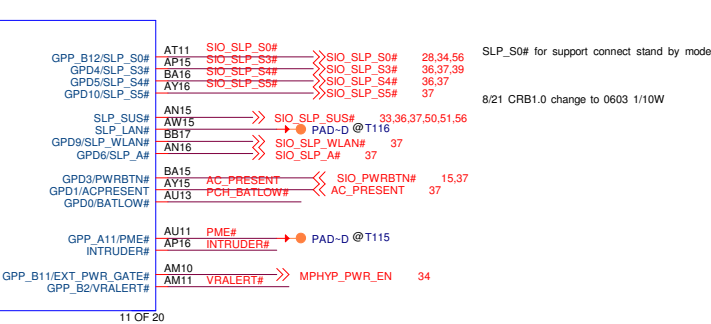
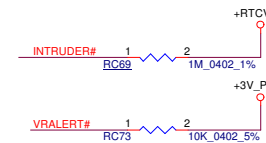
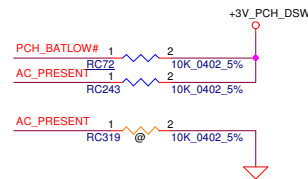
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Size		Document Number			
		P11-MCP(5/14)PCIE,USB,SATA			
		LA-F051P			
Date:		Tuesday, August 01, 2017		Sheet 11 of 57	



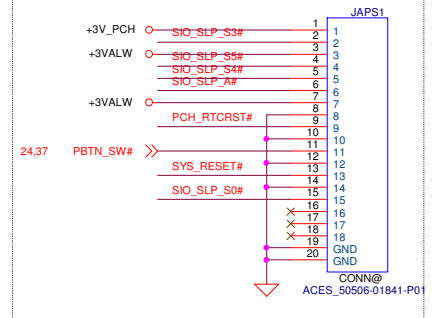
if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)



CMOS1 must take care short & touch risk on layout placement



## APS CONN

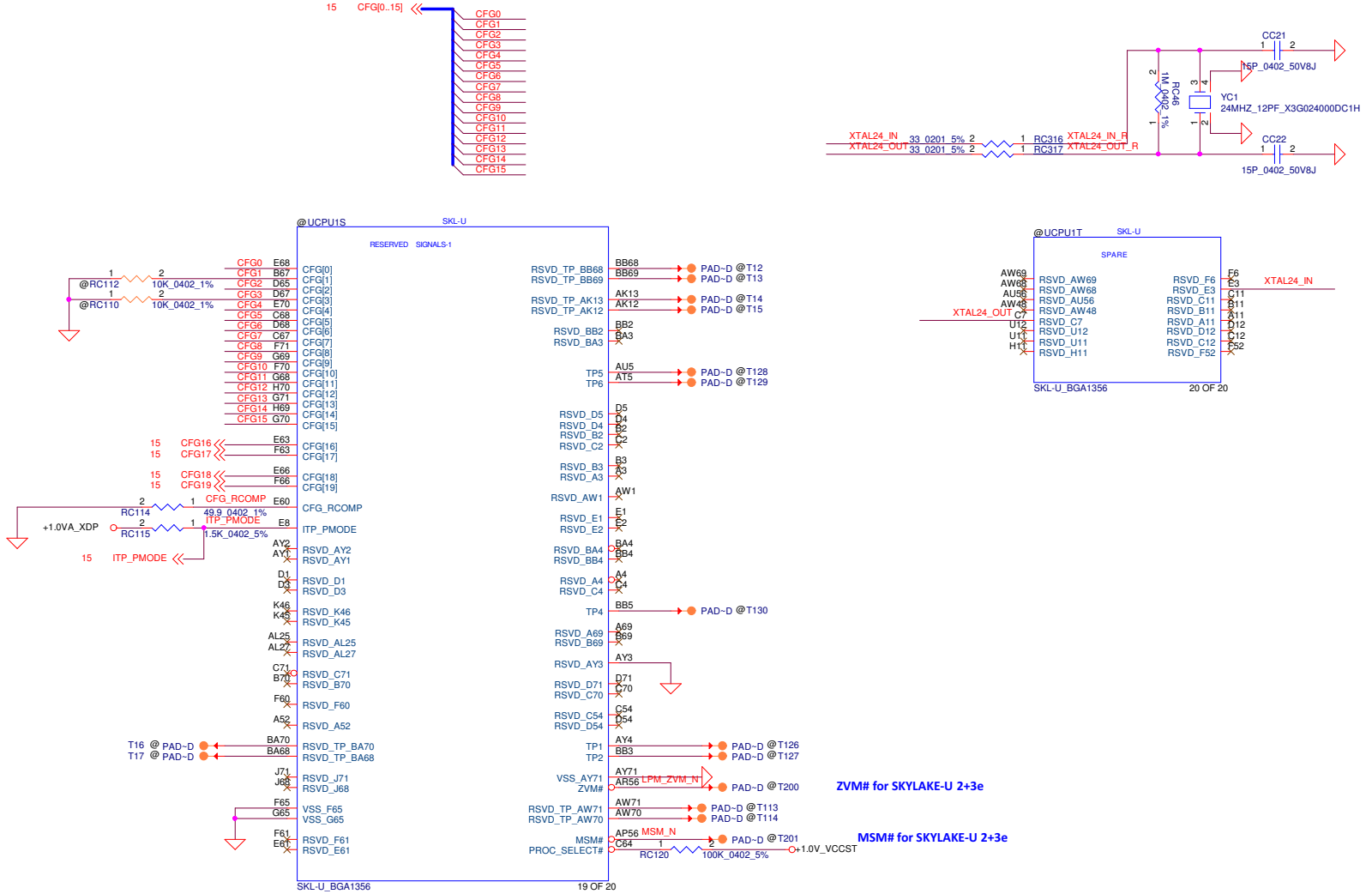
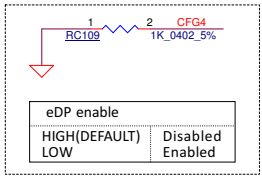
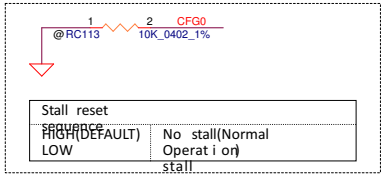


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Title		P12-MCP(6/14)CLK,PM,RTC	
Size	Document Number	LA-F051P	
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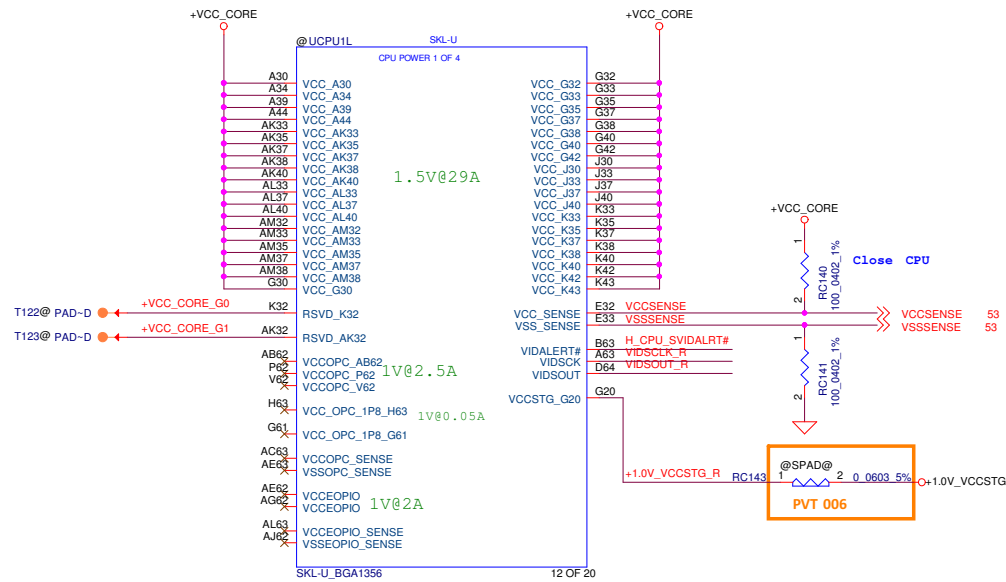




PSC(Primary side cap) : Place as close to the package as possible  
BSC(Backside cap) : Place on secondary side, underneath the package

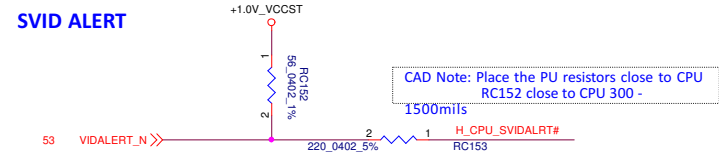
Component placement order:  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC\_CORE: 0.55~1.5V, 64A

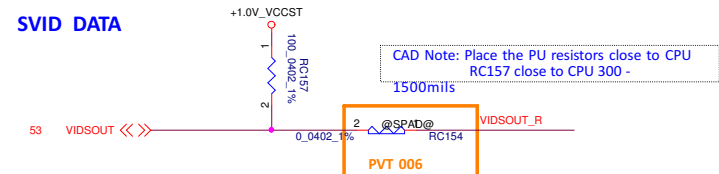


VCCOPC,VCCOPC\_1P8,VCCOEPIO for SKYLAKE-U 2+3e  
(w/ on package cache)

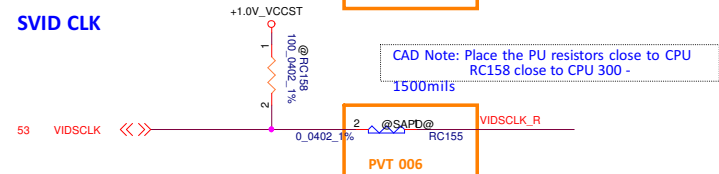
#### SVID ALERT



#### SVID DATA



#### SVID CLK



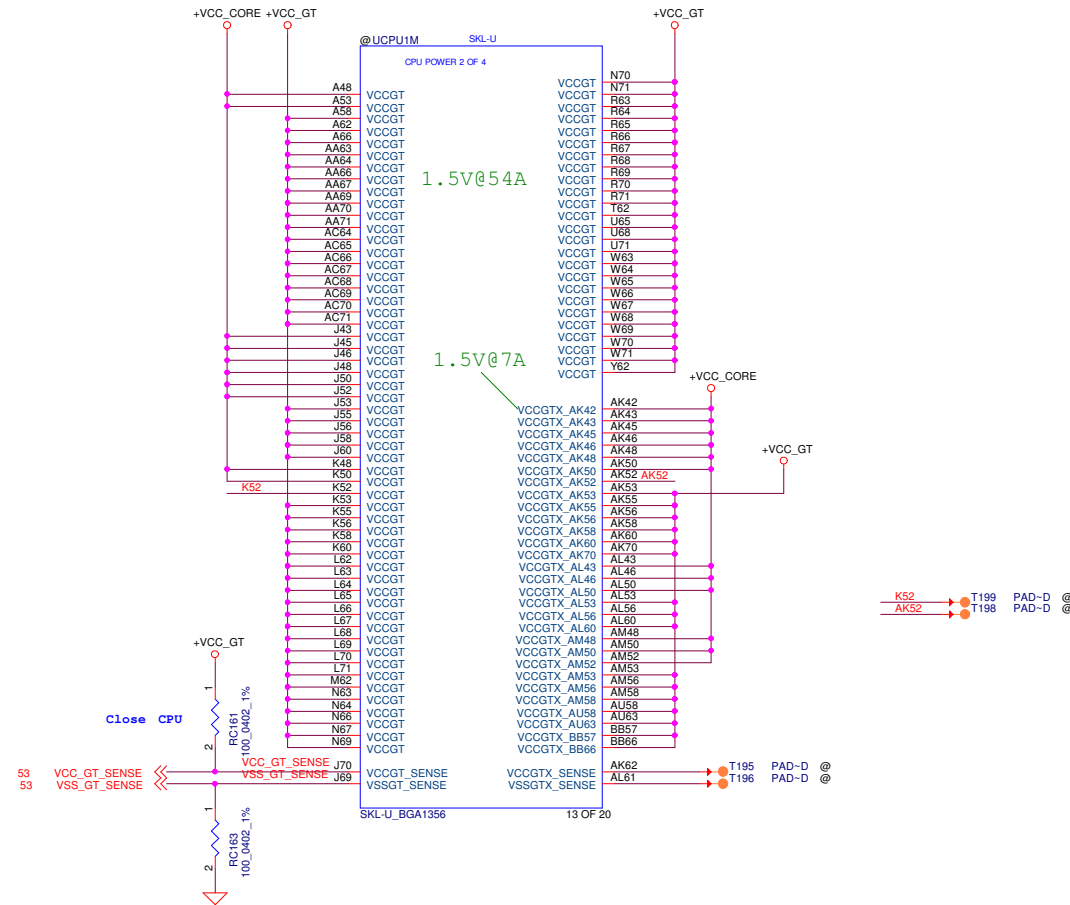
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+VCCGT: 0.55~1.5V, 28A



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P17-MCP(11/14)PWR-VCCGT

Size

Document Number

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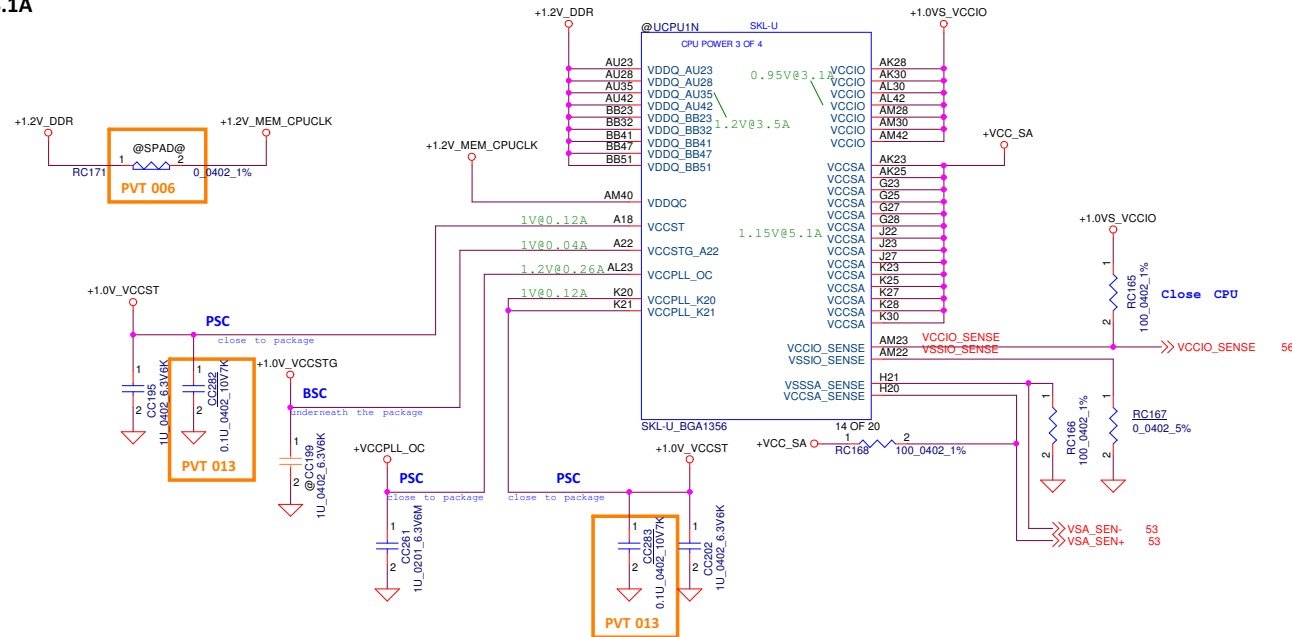
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Date: Tuesday, August 01, 2017

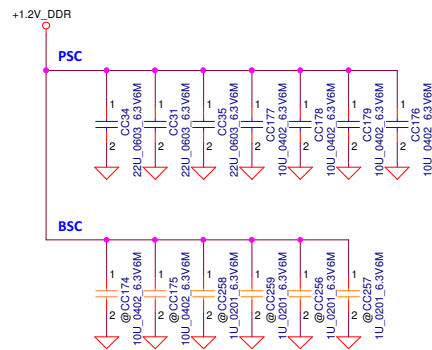
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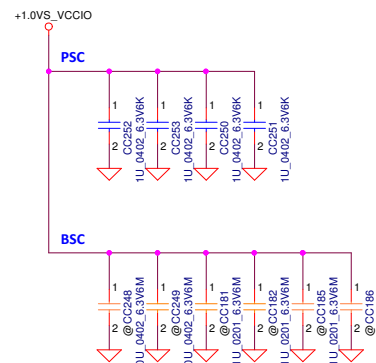
+1.2V\_DDR: 1.2V, 3.5A  
 +1.0V\_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA  
 +1.0V\_VCCSTG: 1V, 40mA  
 +VCCPLL\_OC: 1.2V, 260mA  
 +1.0VS\_VCCIO: 0.85~0.95V, 3.1A  
 +VCC\_SA: 1.15V, 5.0A



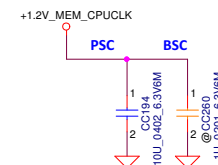
+1.2V\_DDR Decoupling Requirement  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 10U\_0402\*4 pcs + 22U\_0603\*3 pcs



+1.0VS\_VCCIO Decoupling Requirement  
 Back Side (underneath the package):  
 10U\_0402\*2 pcs + 1U\_0201\*4 pcs (8)  
 Primary Side (close to package):  
 1U\_0402\*4 pcs



+1.2V\_MEM\_CPUCLK (VDDQC) Place on CPU  
 Back Side (underneath the package):  
 1U\_0201\*1 pcs (8)  
 Primary Side (close to package):  
 10U\_0402 \* 1 pcs

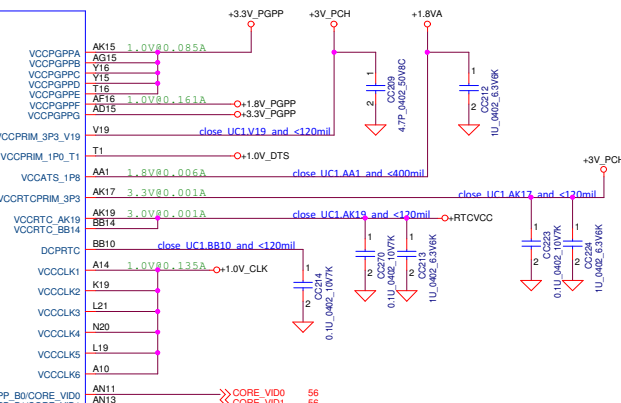
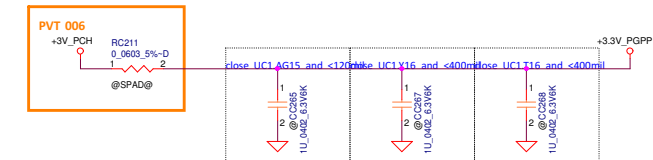
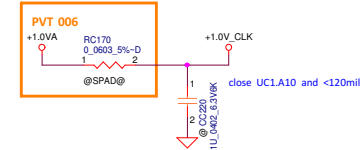
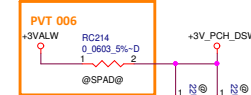
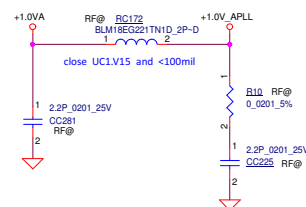
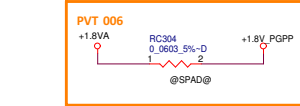
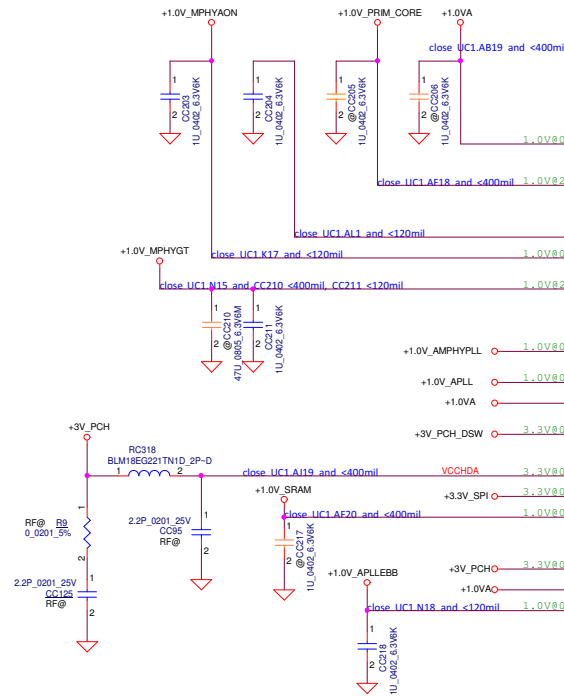
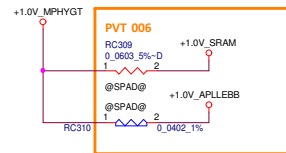
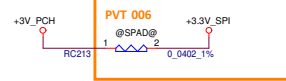
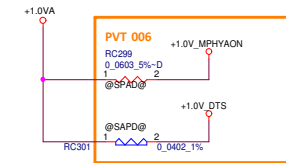
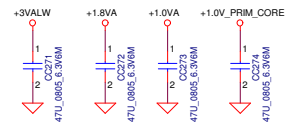


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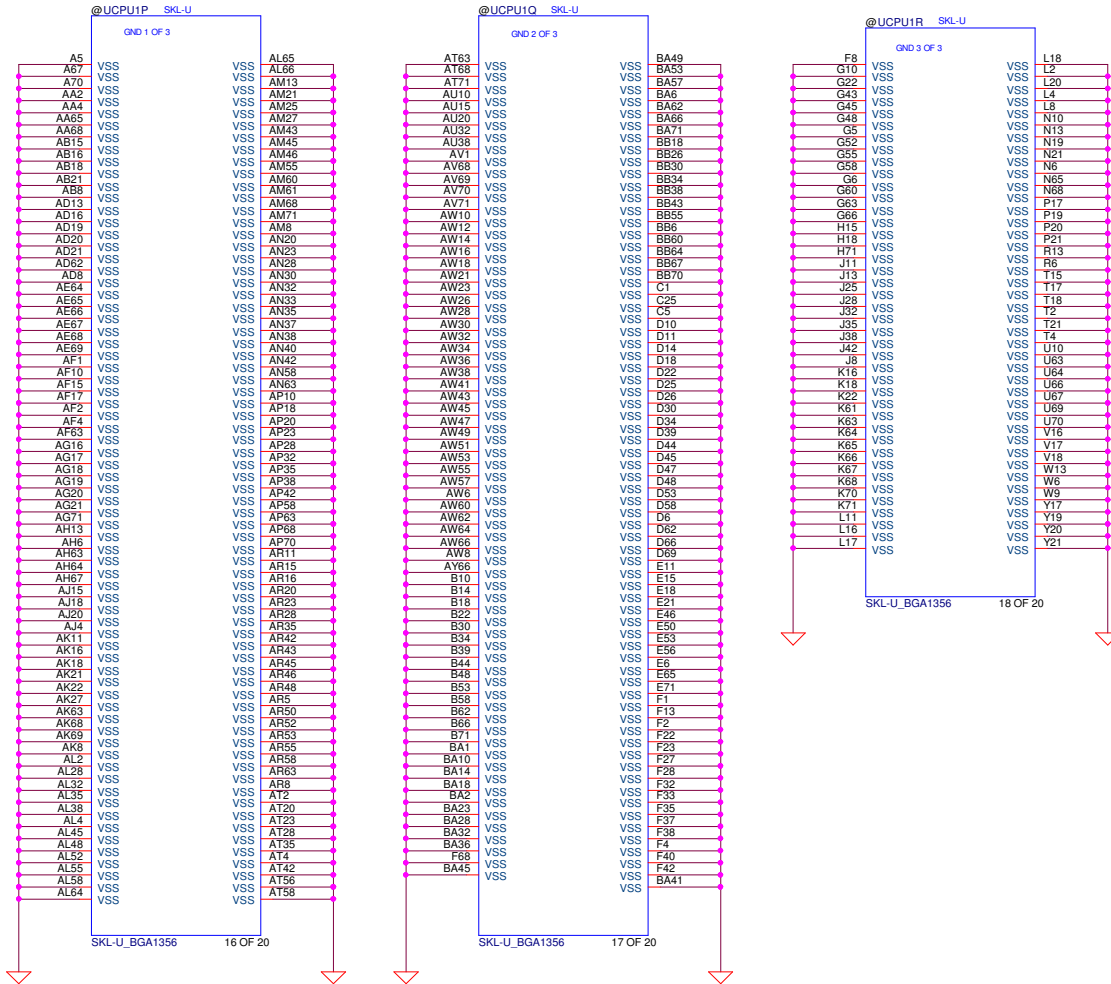
Title	P18-MCP(12/14)PWR-VCCIO, MEM	
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Take care!!! Note1 on Page 19

Note1: VCCPRIM\_CORE Implementat i on w t h PCH CORE\_V D Reco mnendati on

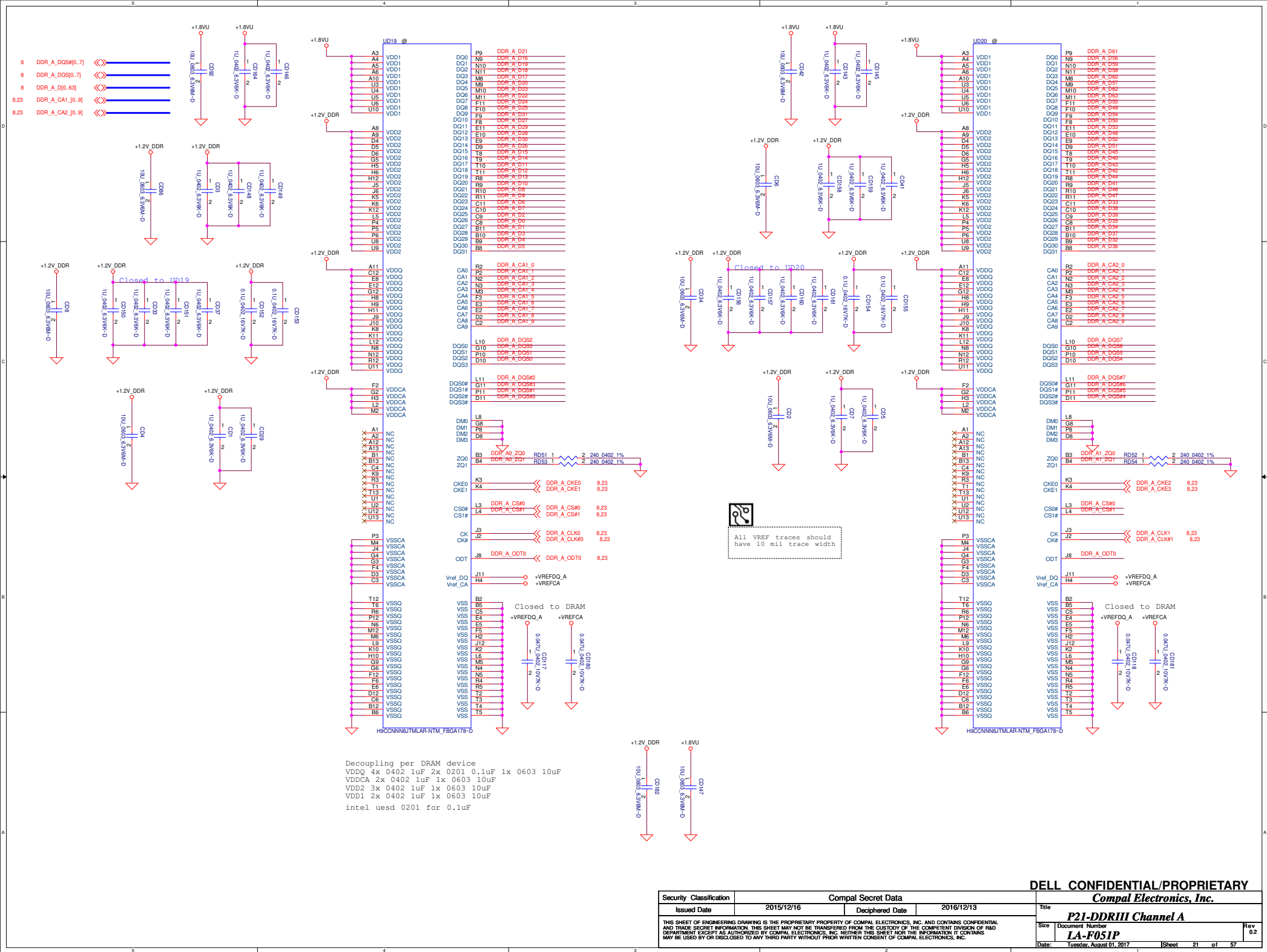
R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



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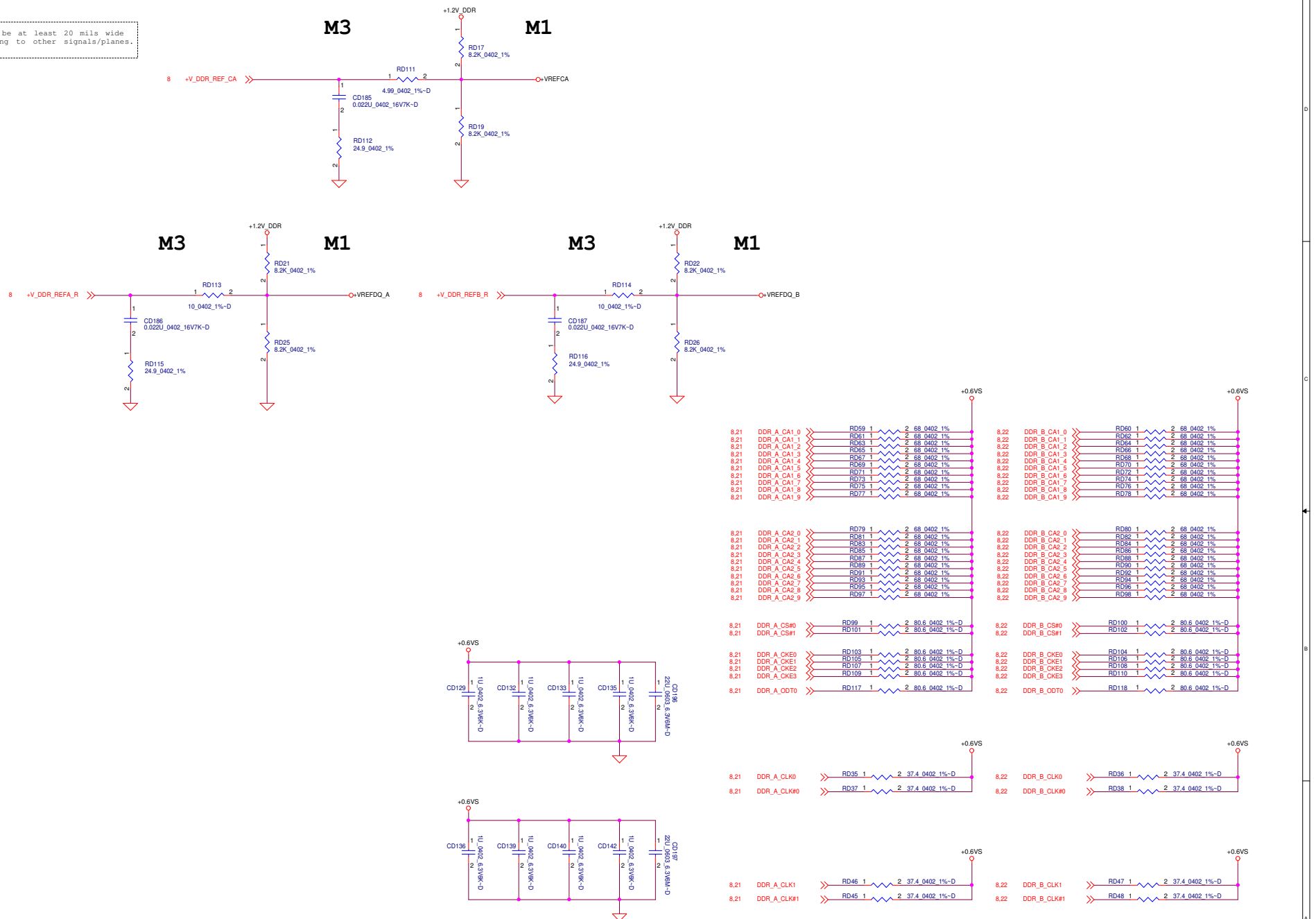
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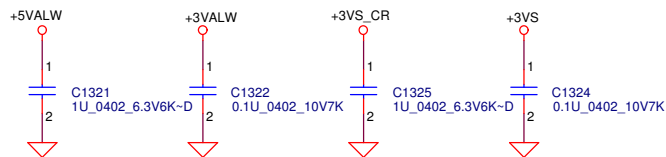




VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.



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							P23-DDRIII Vref & Termination
							Size
							Document Number
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11 PCIE\_PTX\_CARDRX\_P6 >> CH13 1  
11 PCIE\_PTX\_CARDRX\_N6 >> CH14 1

11 USB3RN1 <<  
11 USB3RP1 <<  
11 USB3TN1 <<>>  
11 USB3TP1 <<>>

2 0.1U 0402 10V7K-D PCIE\_PTX\_CARDRX\_P6\_C  
2 0.1U 0402 10V7K-D PCIE\_PTX\_CARDRX\_N6\_C

38 USB\_PWR\_SHR\_EN\_R# >>  
12 CLK\_PCIE\_MMI >>  
12 CLK\_PCIE\_MMI# >>  
11 USB\_OC1# <<

11 PCIE\_PRX\_CARDTX\_P6 <<  
11 PCIE\_PRX\_CARDTX\_N6 <<

12 CLKREQ\_PCIE#5 >>  
11 USB20\_P1 <<>>

11 USB20\_N1 <<>> PBTN\_SW#  
12,37 PBTN\_SW# <<>>

37 USB1\_DET# <<>>  
10 HOST\_SD\_WP# <<>>  
12,28,29,30,37,39 PCH\_PLTRST#\_EC <<>>  
38 USB\_PWR\_SHR\_VBUS\_EN\_R <<>>

37 BREATH\_LED# <<>>  
9 MEDIACARD\_IRQ# <<>>  
37 LID\_SW\_IN# <<>>

+3VS\_CR

+3VALW

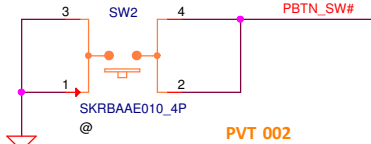
+3VS

+5VALW

J101

JXT\_FP270H-061G1AM  
CONN@

### NPI Stage Power Switch



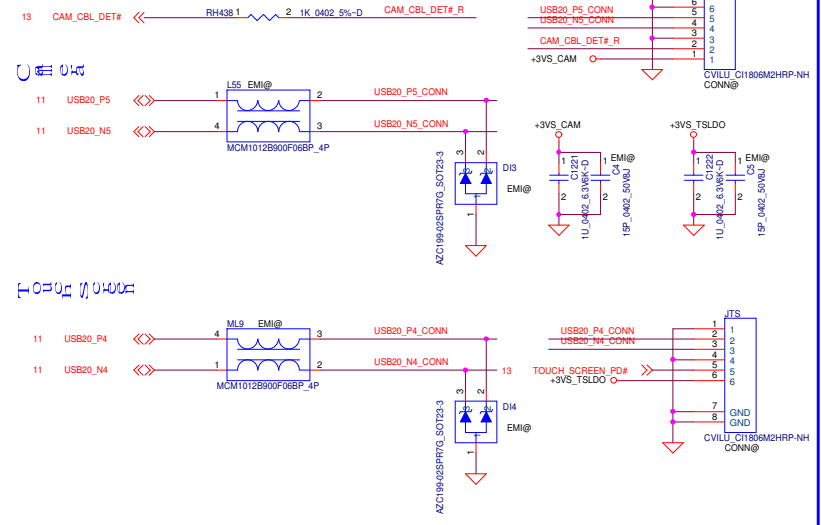
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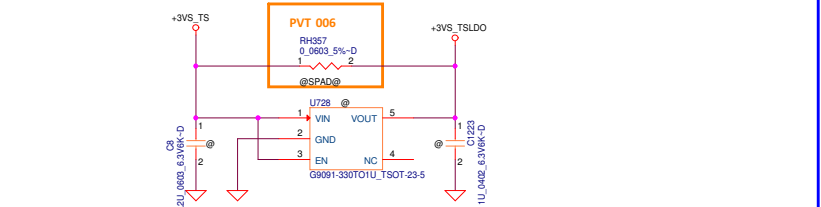
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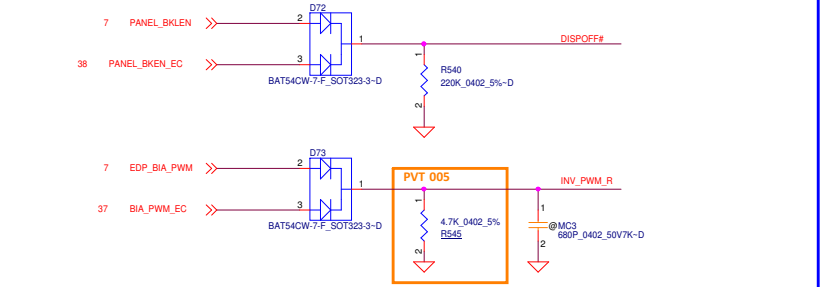
USB + Power Schematic



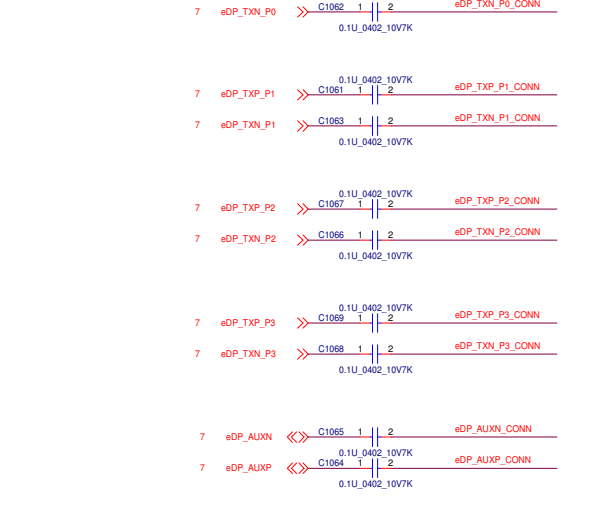
Power Schematic



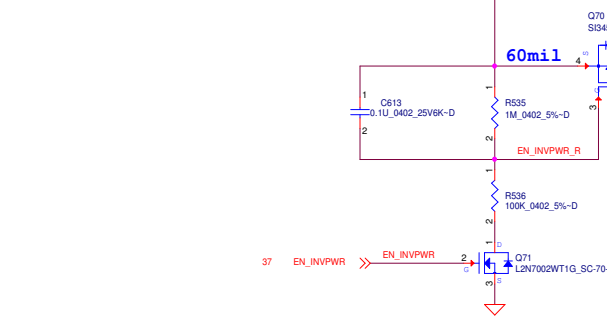
Backlight LED Schematic



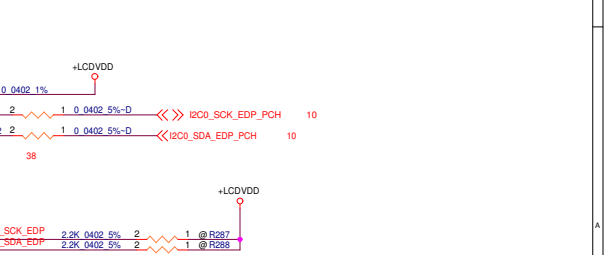
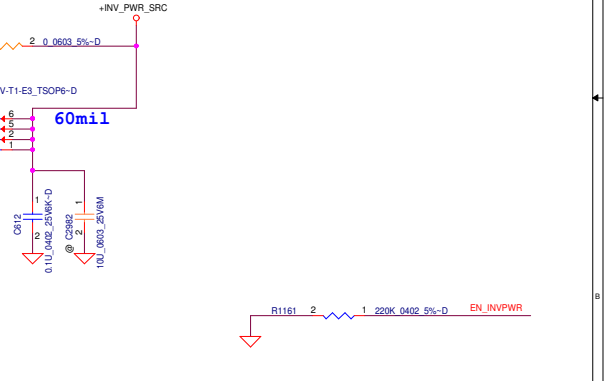
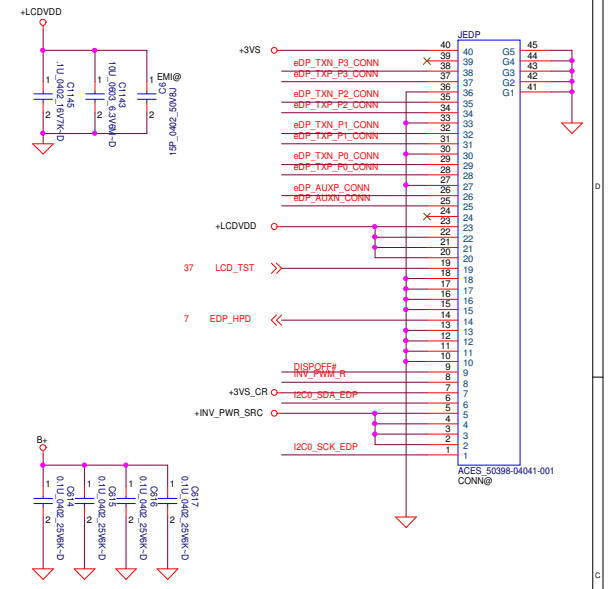
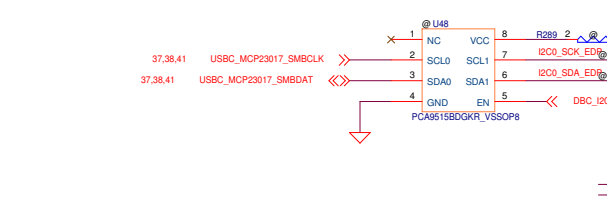
DP Schematic

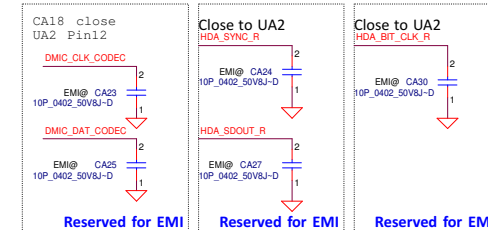
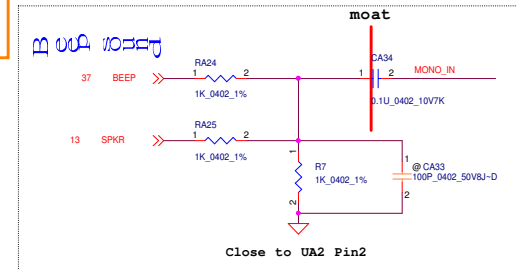
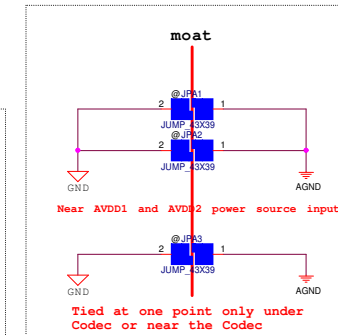


DP Backlight LED Schematic

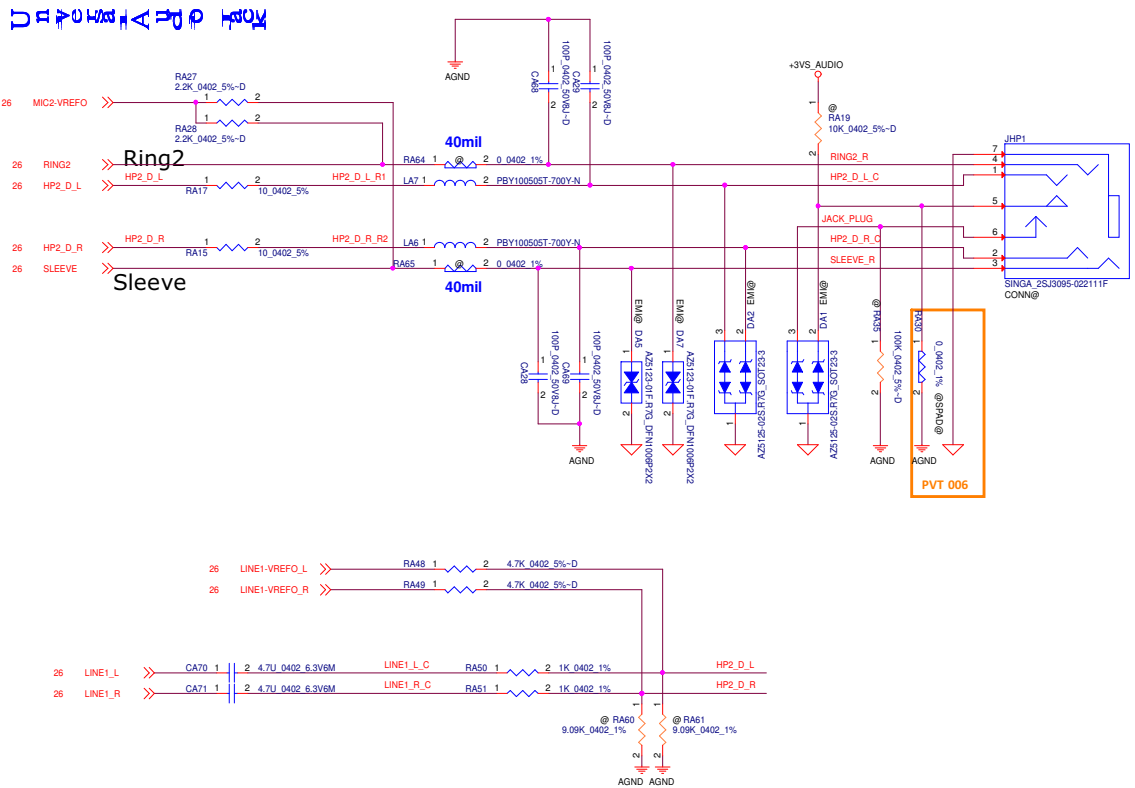


DP Schematic

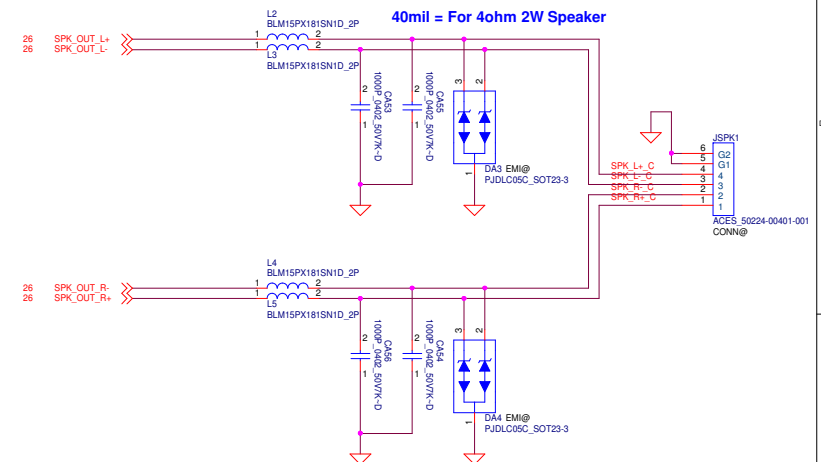




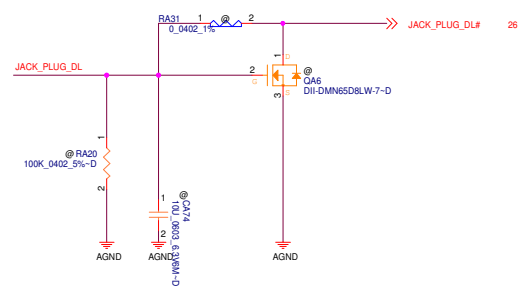
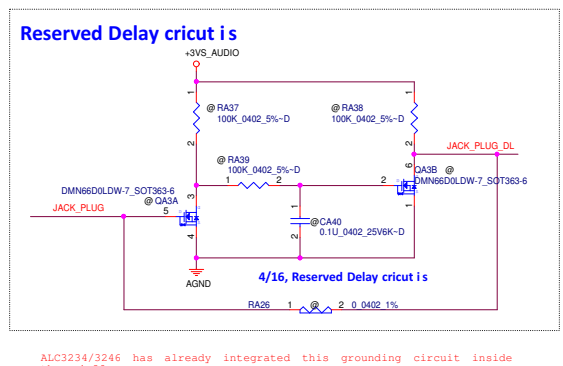
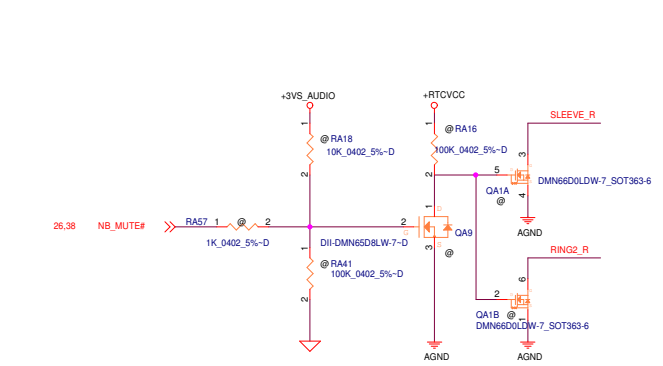
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## HF: SPOXYEPOXY



• **Not a good idea to use a single variable to represent a categorical variable.**

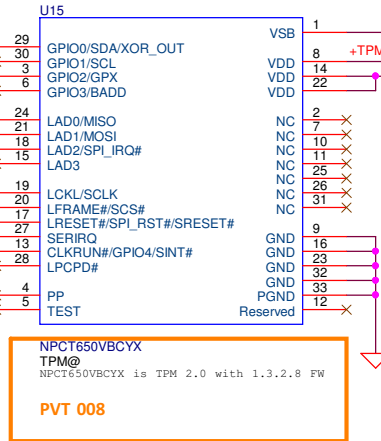
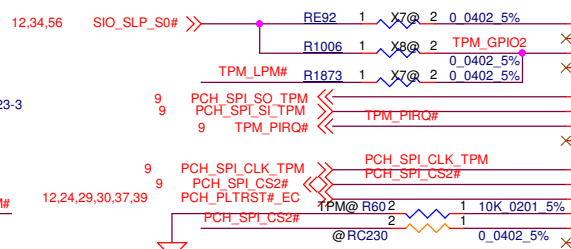
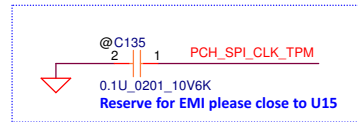
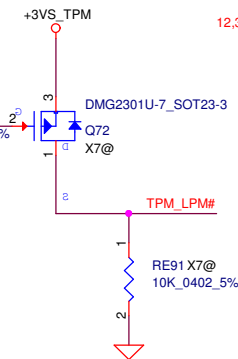
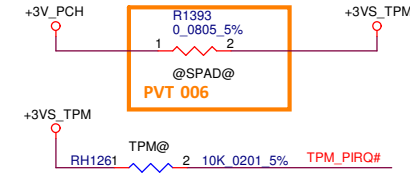


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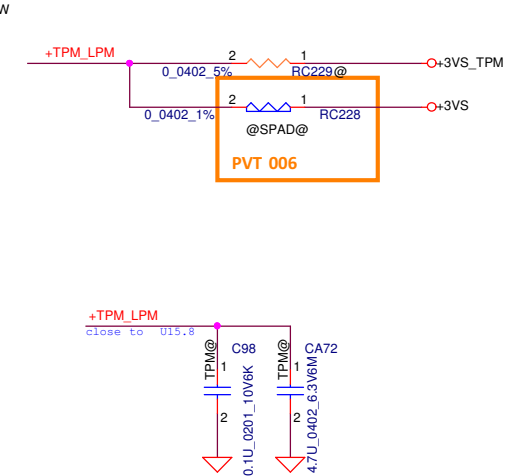
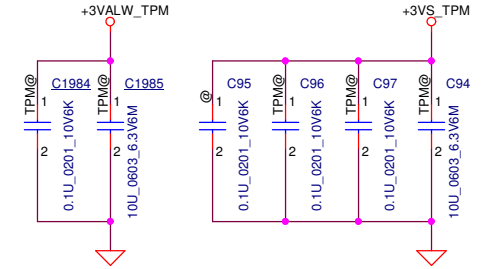
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# TPM

NOTE:  
Follow the SPI topology layout guidelines  
in the relevant Intel Platform Design Guide



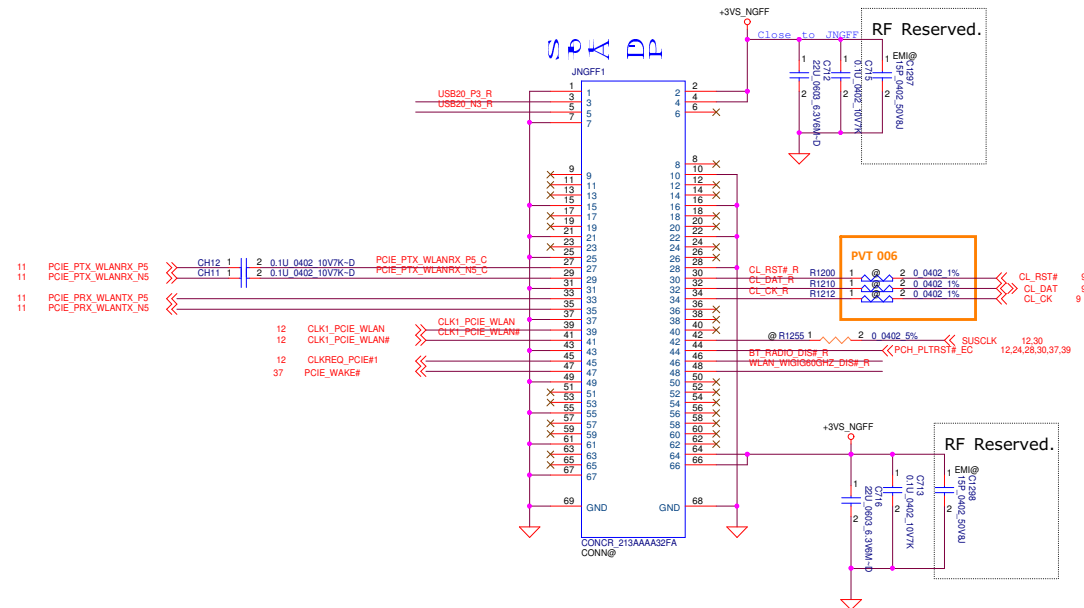
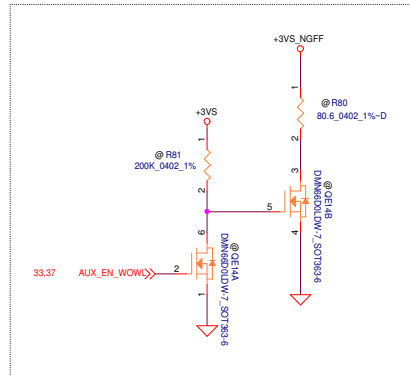
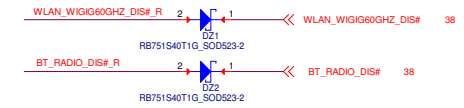
NOTE:  
Place 0.1 uF capacitors as close as  
possible to the device power pins



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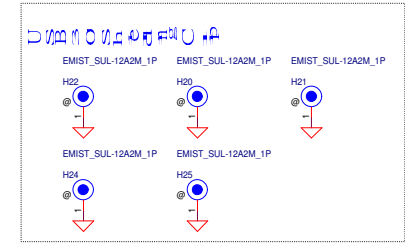
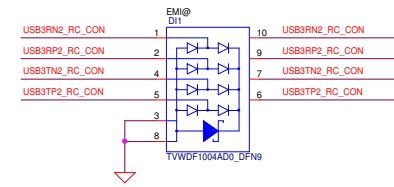
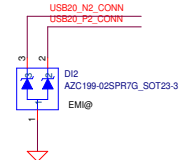
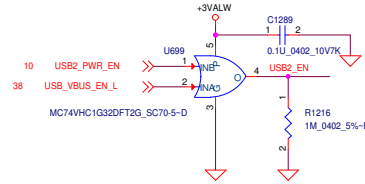
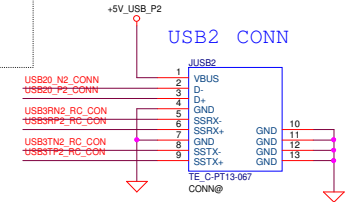
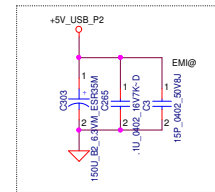
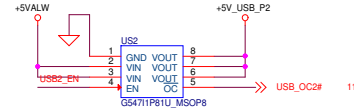
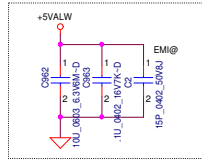
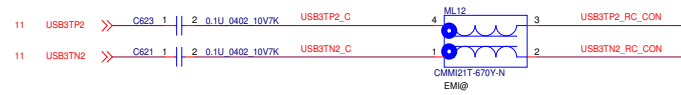
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				LA-F051P	
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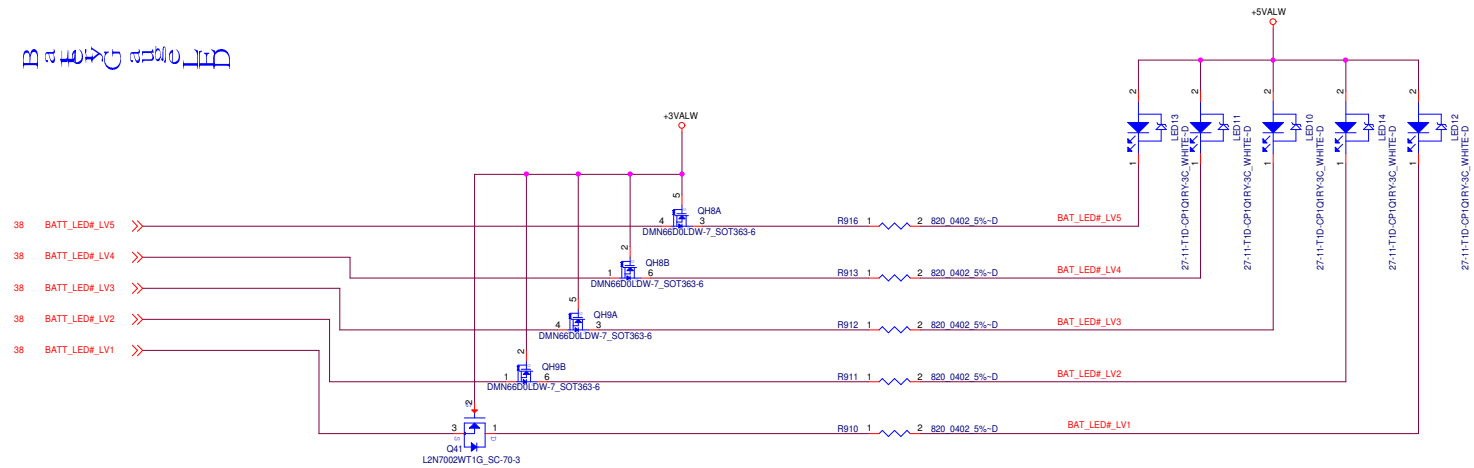


COMPAL

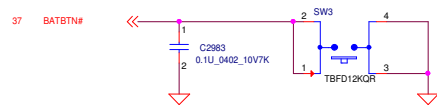


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Deciphered Date				2016/12/13				P31-USB 3.0 IO CONN			
Title				Document Number				LA-F051P			
Size				Sheet				31 of 57			
Date:				Tuesday, August 01, 2017				Rev 0.2			

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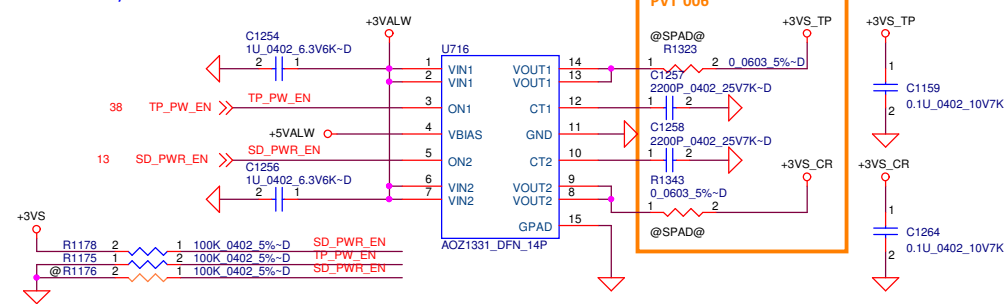


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Compal Electronics, Inc.

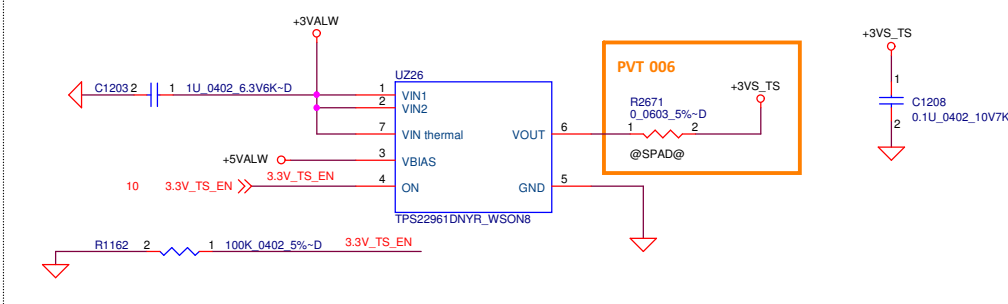
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Issued Date	2015/12/16	Deciphered Date	2016/12/13
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Size	32	of	57
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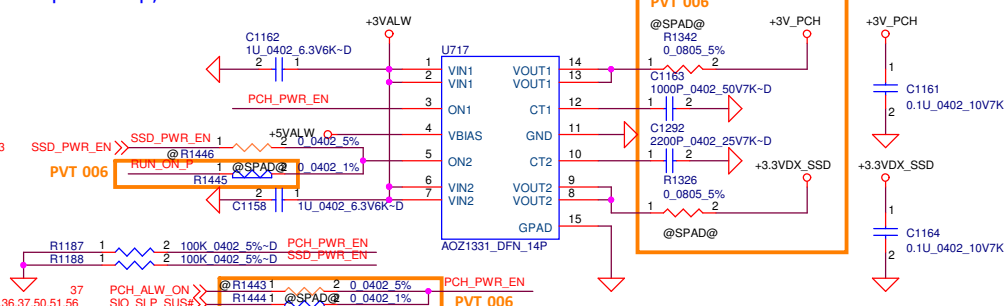
## Touch Pad, Card Reader Load Switch



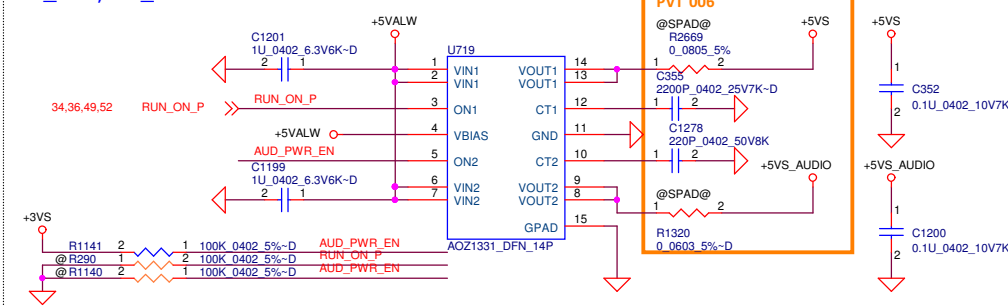
## Touch Screen Load Switch



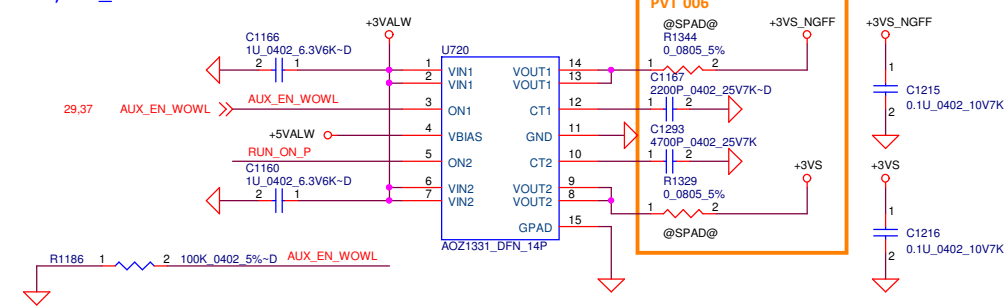
## Deeper Sleep, SSD Load Switch



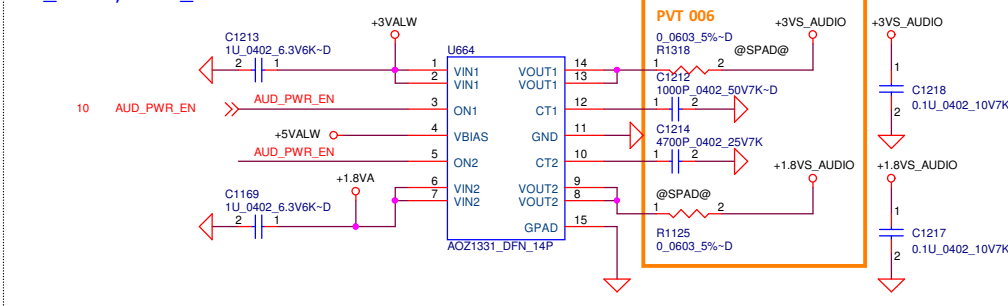
## 5V\_Run, 5V\_Audio Load Switch



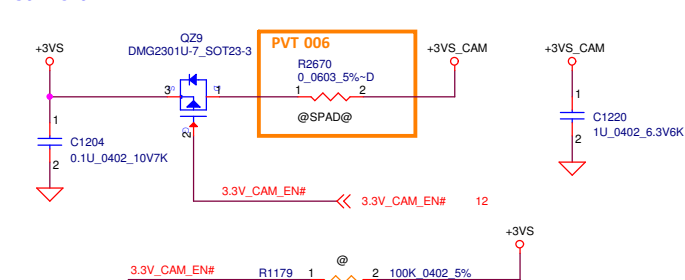
## WiFi, 3V\_RUN Load Switch



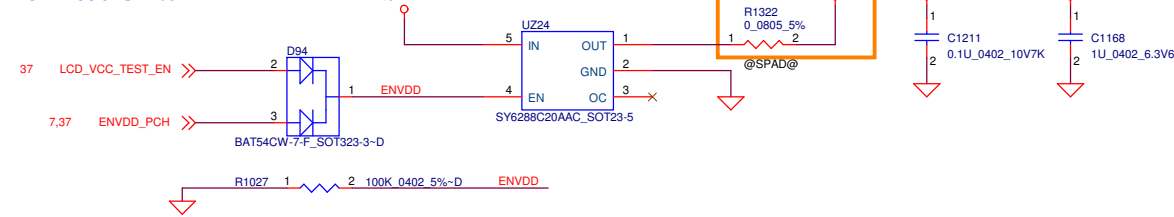
## 3V\_Audio, 1.8V\_Audio Load Switch



## Camera



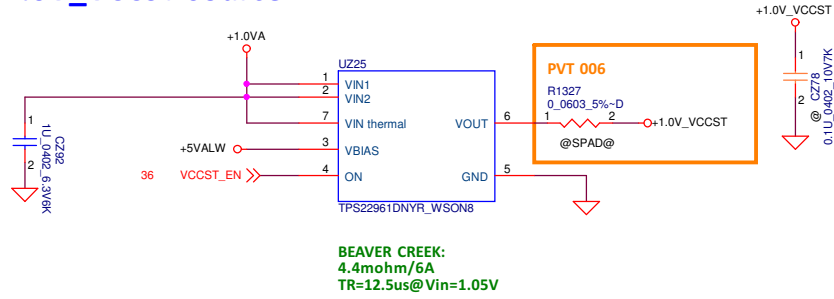
## LCD Load Switch



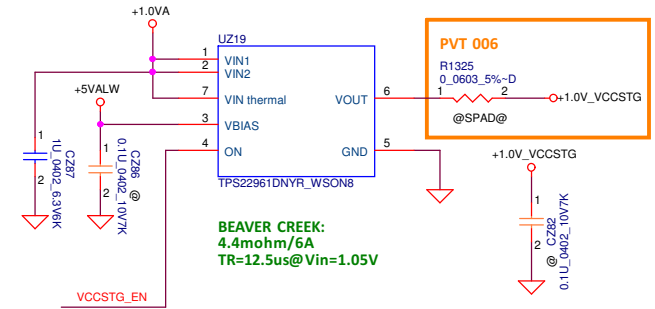
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								P33-DC/DC Interface 1			
								Size			
								Document Number			
								LA-F051P			
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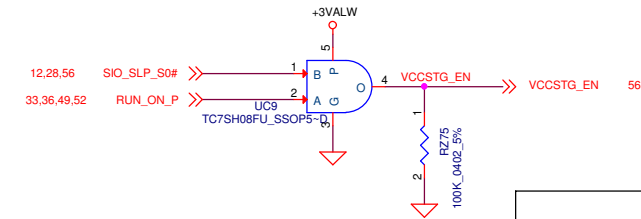
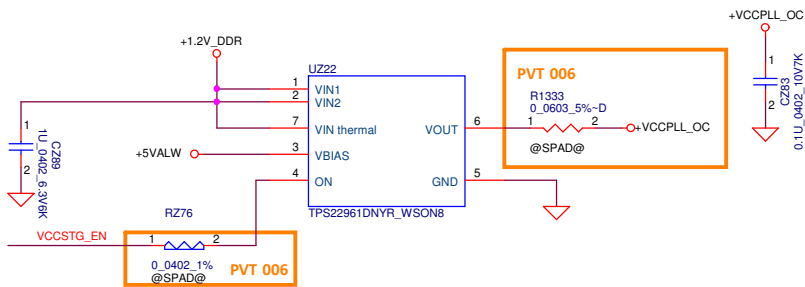
## +1.0V\_VCCST source



## +1.0V\_VCCSTG source

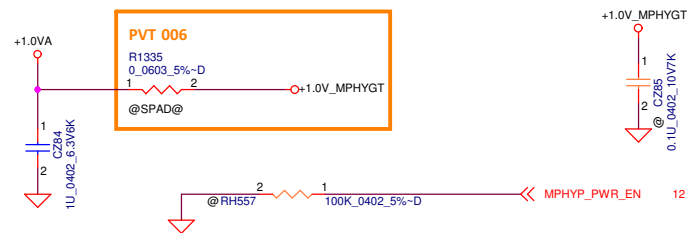


## +VCCPLL\_OC source

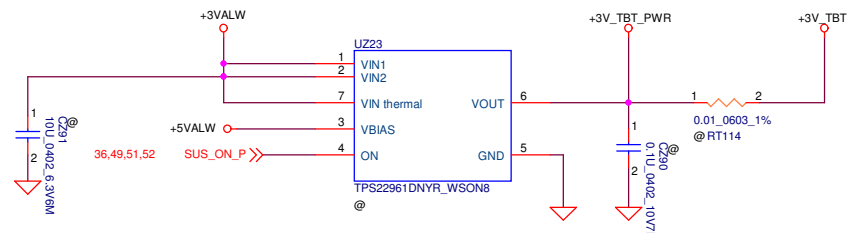


	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

## +1.0V\_MPHYGT source

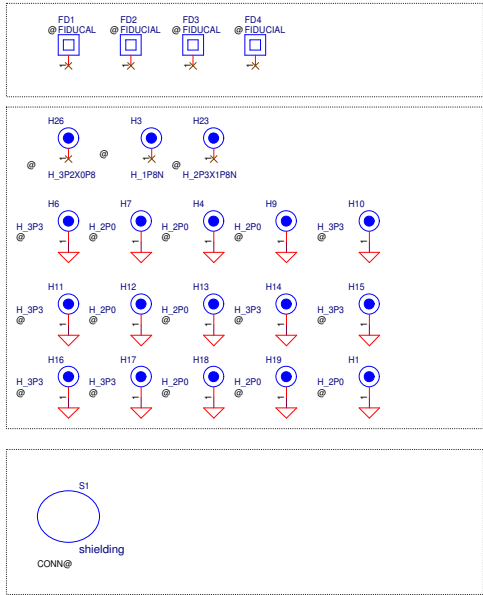


## TBT Power circuits

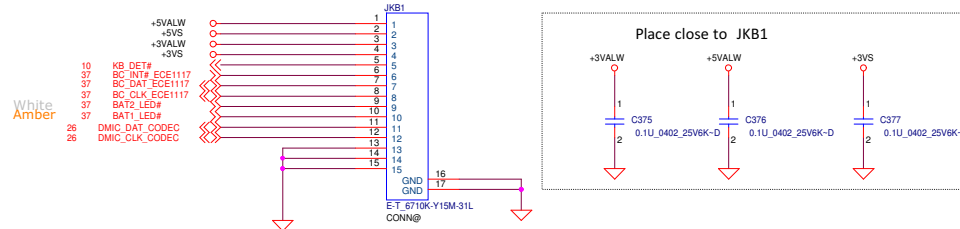


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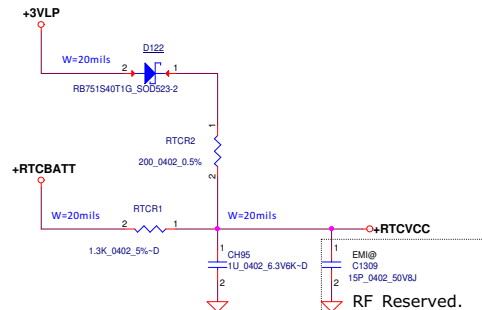
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Title <b>P34-DC/DC Interface 2</b>			
Size	Document	Number	Rev
		<b>LA-F051P</b>	0.2
Date:	Tuesday, August 01, 2017	Sheet	34 of 57



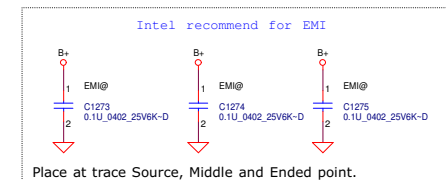
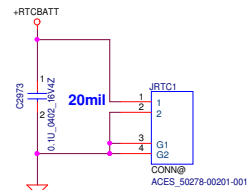
## Keyboard Controller board + DMIC



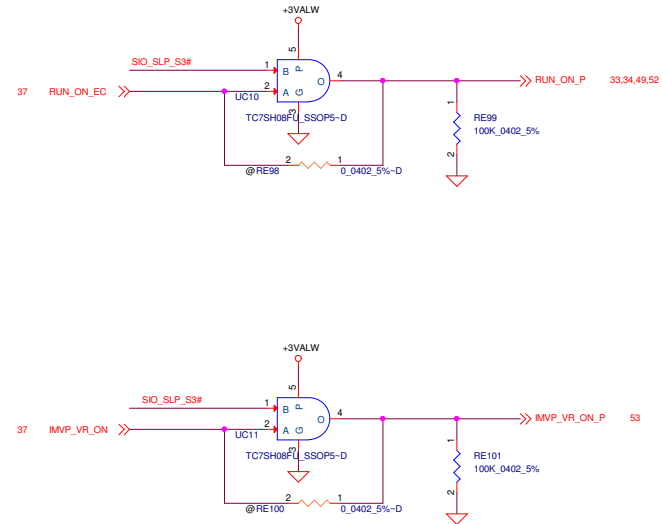
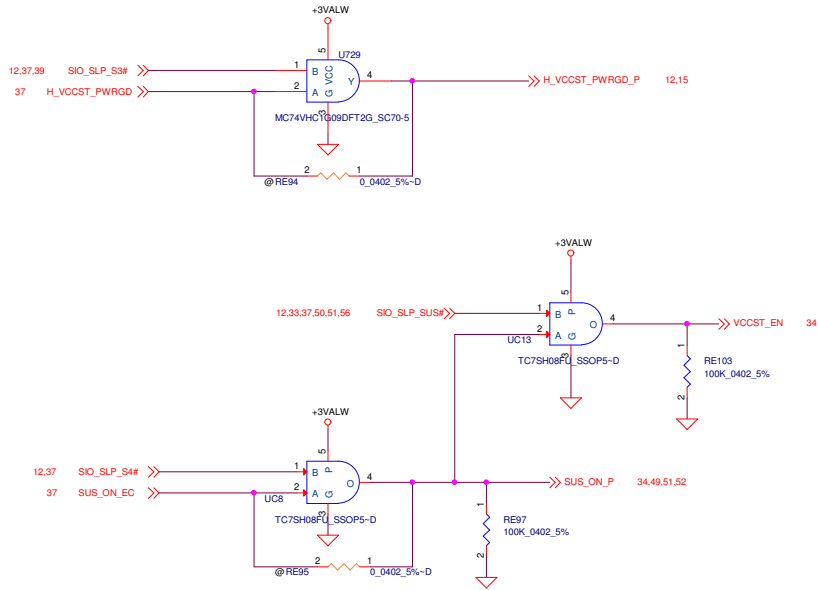
## RTC Battery With Charge Function



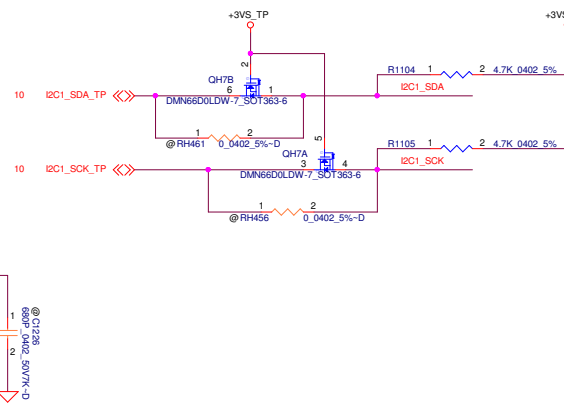
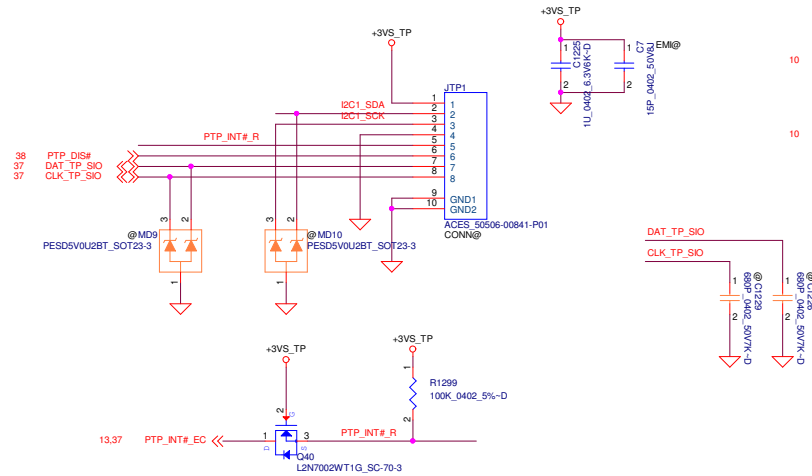
## RTC Battery Conn



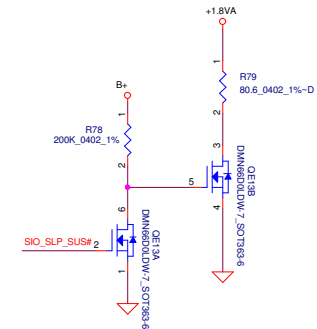
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				Size	Document Number
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## Touchpad CONN

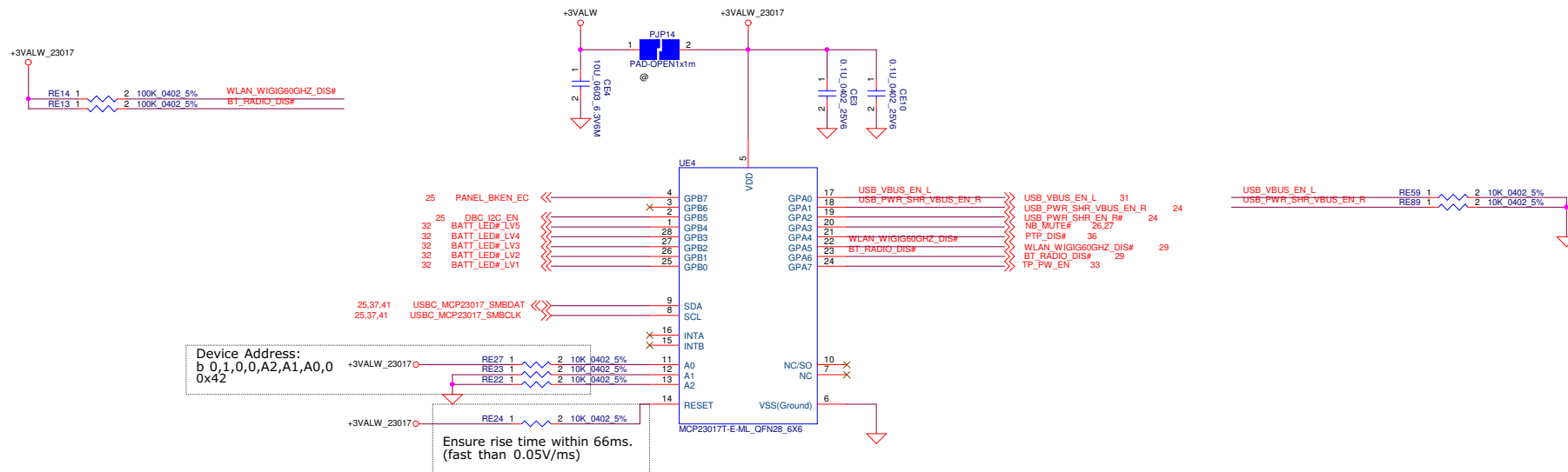


## +1.8VA Discharge



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Title	P36-TP/PWGRGD/LID		
Size	Document Number	Rev	
	LA-F051P	0.2	
Date:	Tuesday, August 01, 2017	Sheet	36 of 57

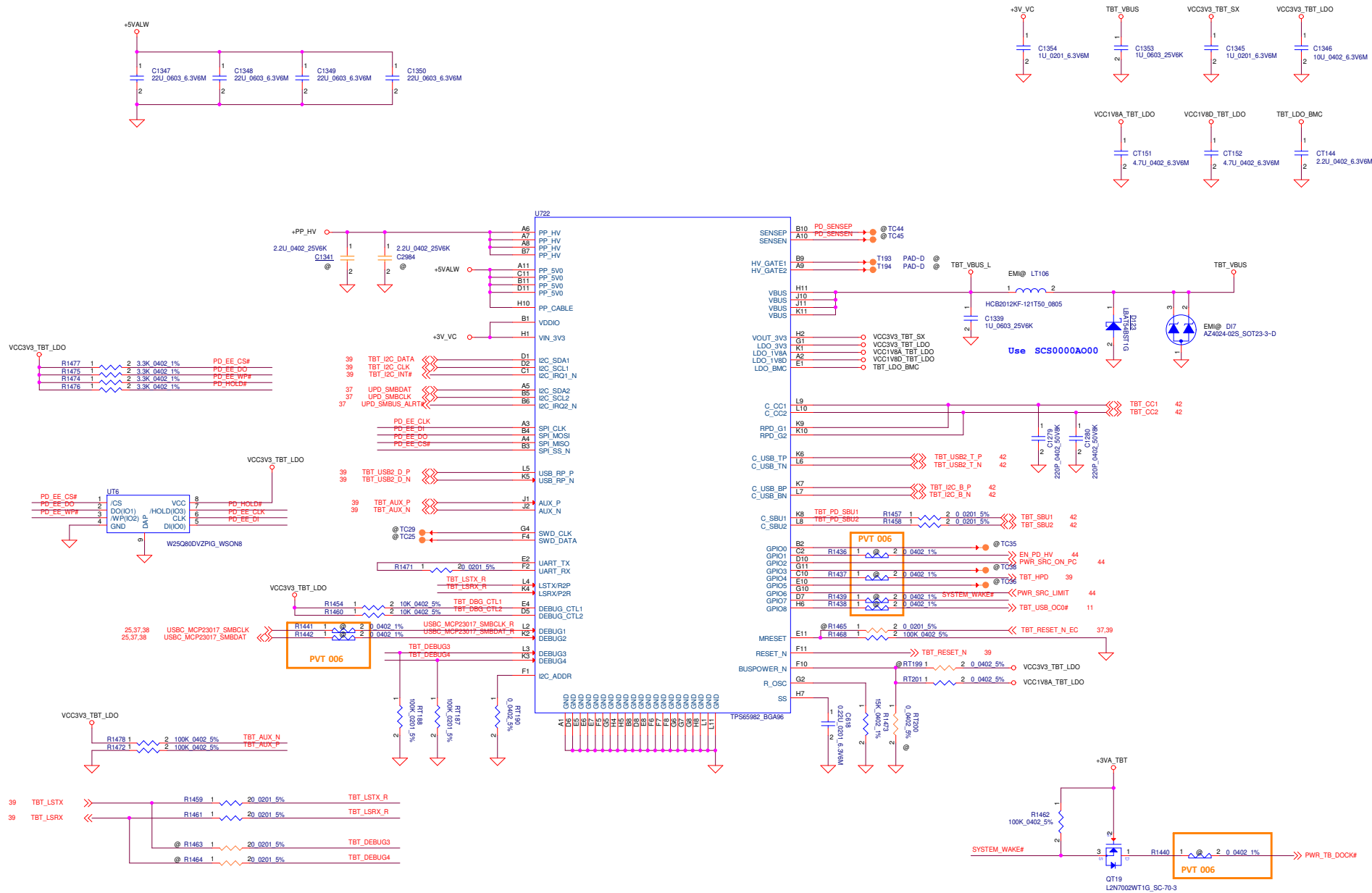


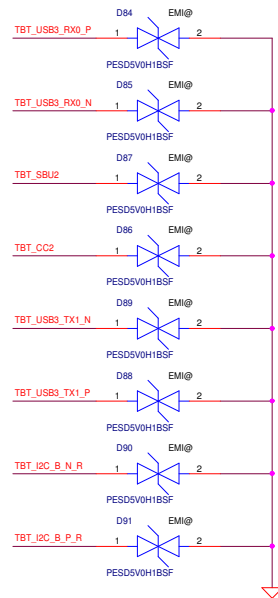
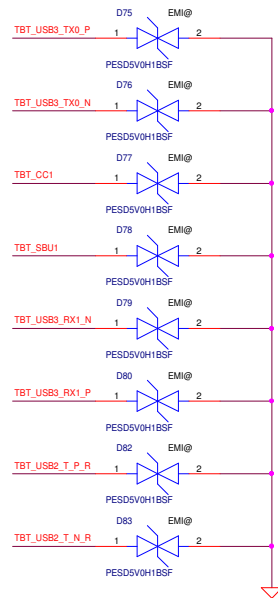
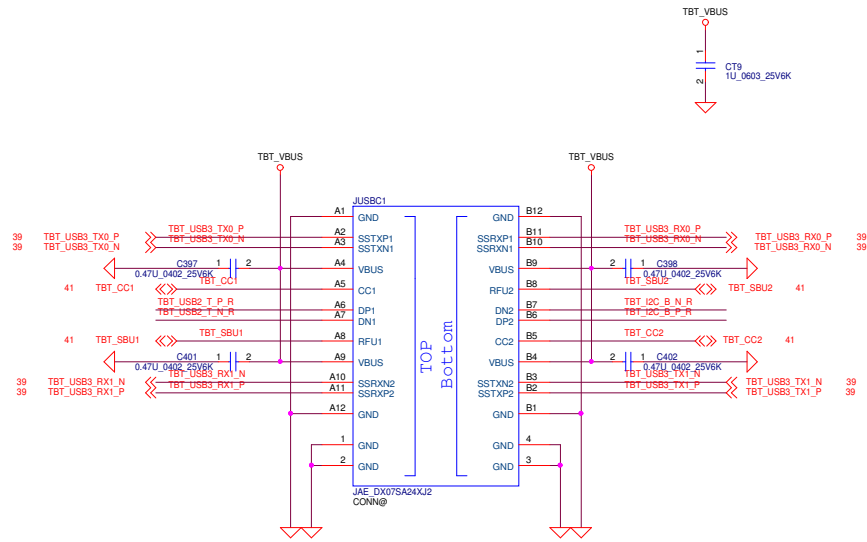
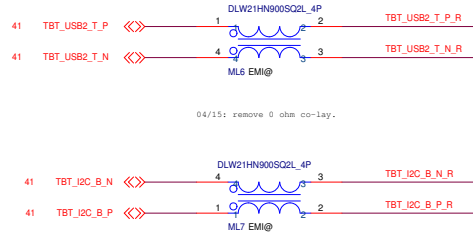


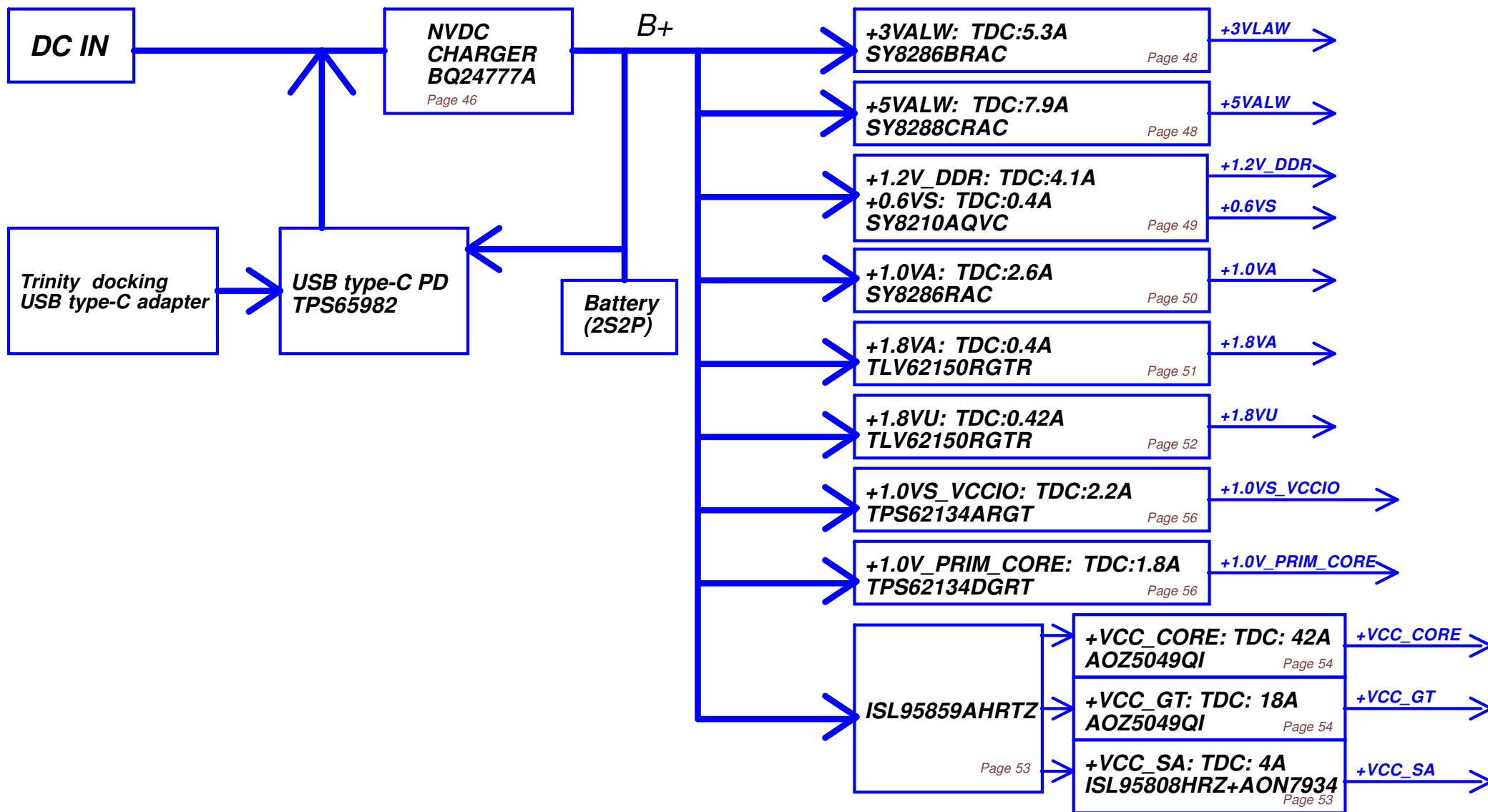






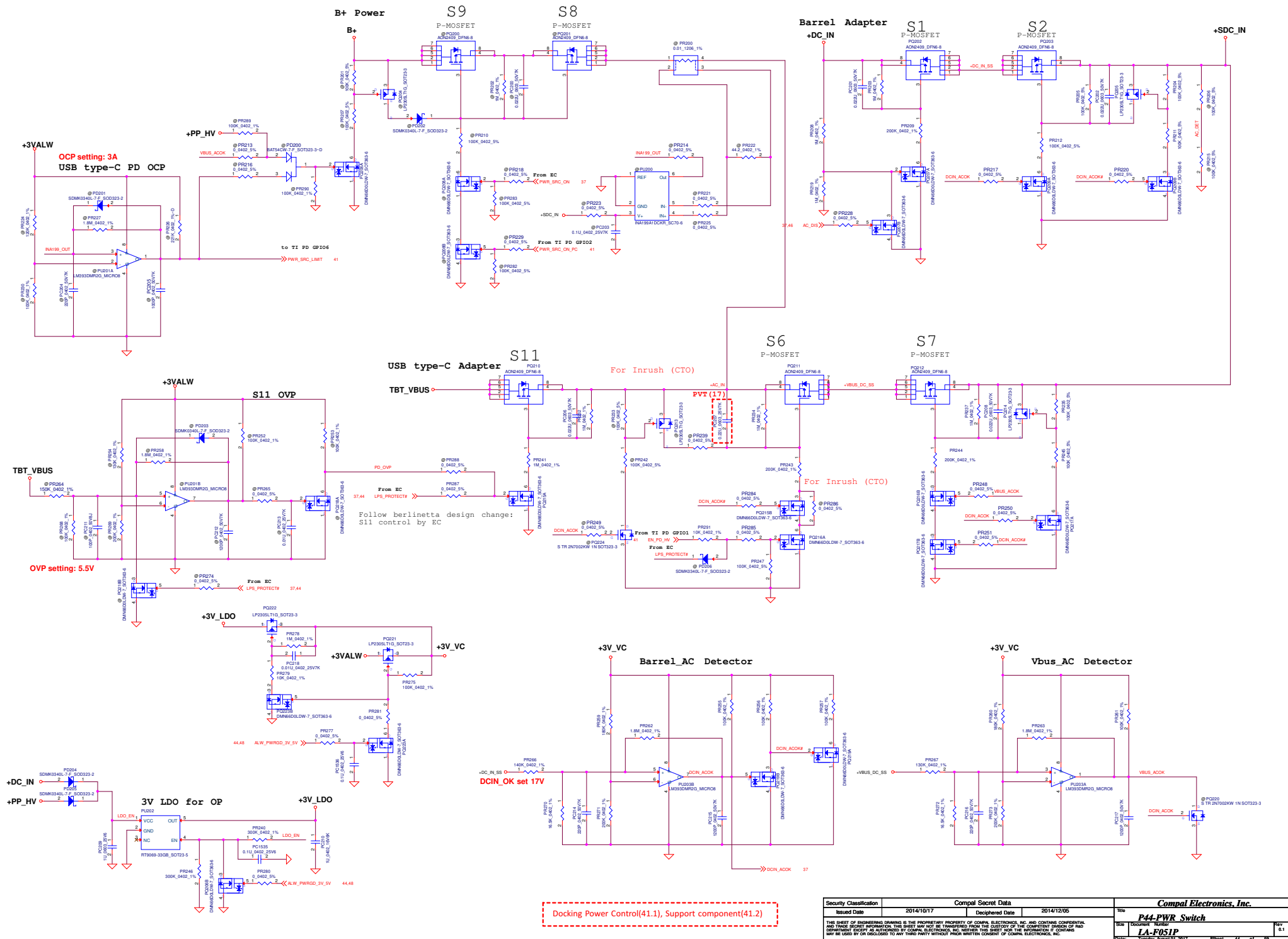






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						P43-PWR Block Diagram				
						Size	Document Number			
						LA-F051P				Rev 0.1
Date:		Tuesday, August 01, 2017		Sheet	43	of 59				

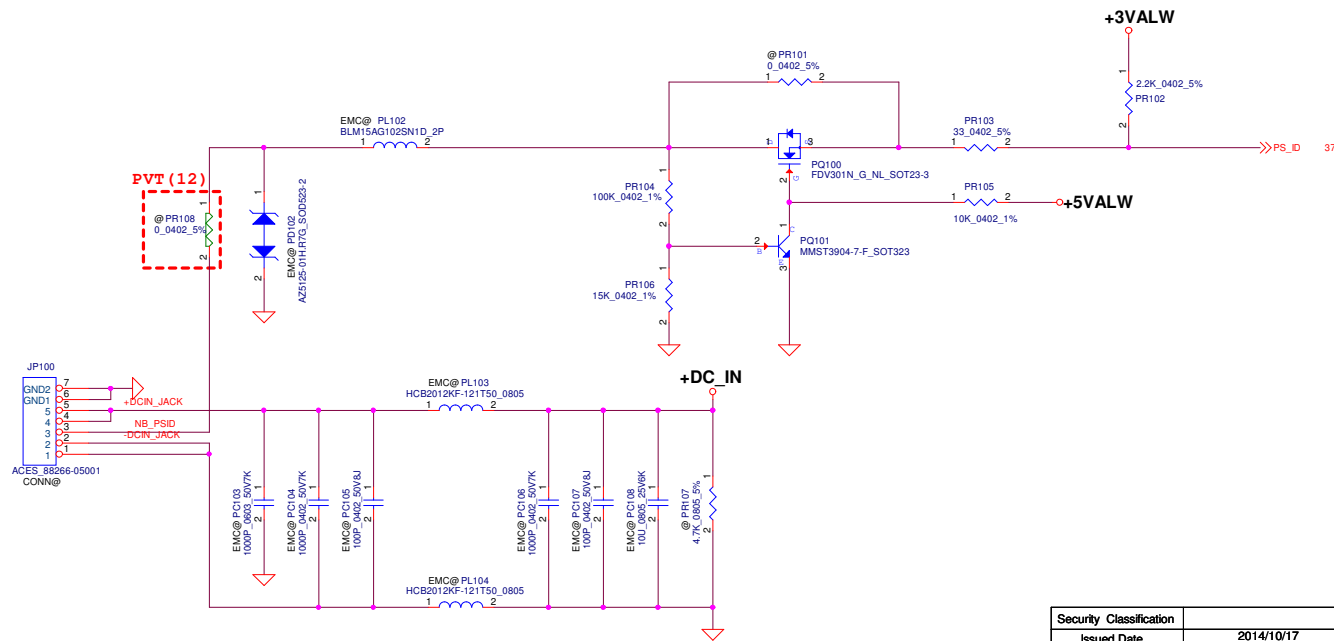
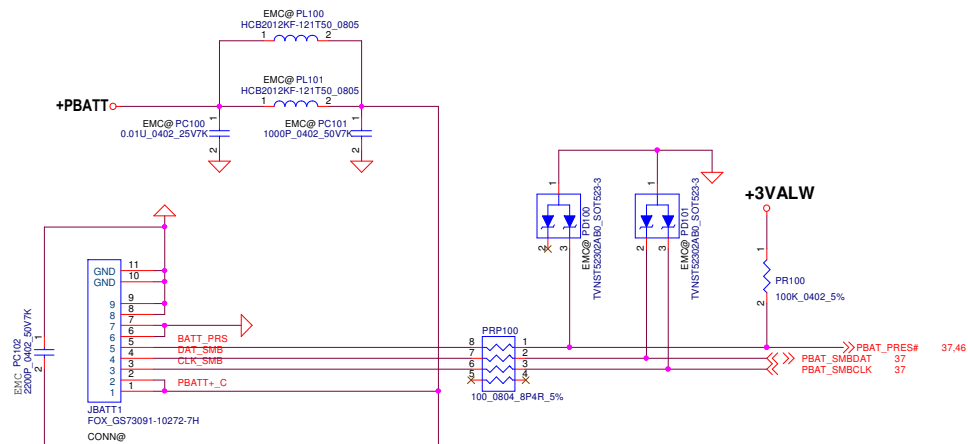
Remove source back function



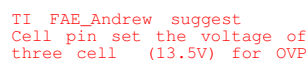
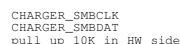
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Issued Date		Deciphered Date		P4-PWR Switch	
2014/10/17		2014/12/05		LA-F051P	
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2014/12/05		2014/12/05		44	

# PBATT1 connector

SMART  
Battery:  
1.BATT++  
2.BATT++  
3.CLK\_SMB  
4.DAT\_SMB  
5.BAT\_PRS  
6.SYS\_PRES  
7.BAT\_ALERT  
8.GND  
9.GND  
10.GND  
11.GND

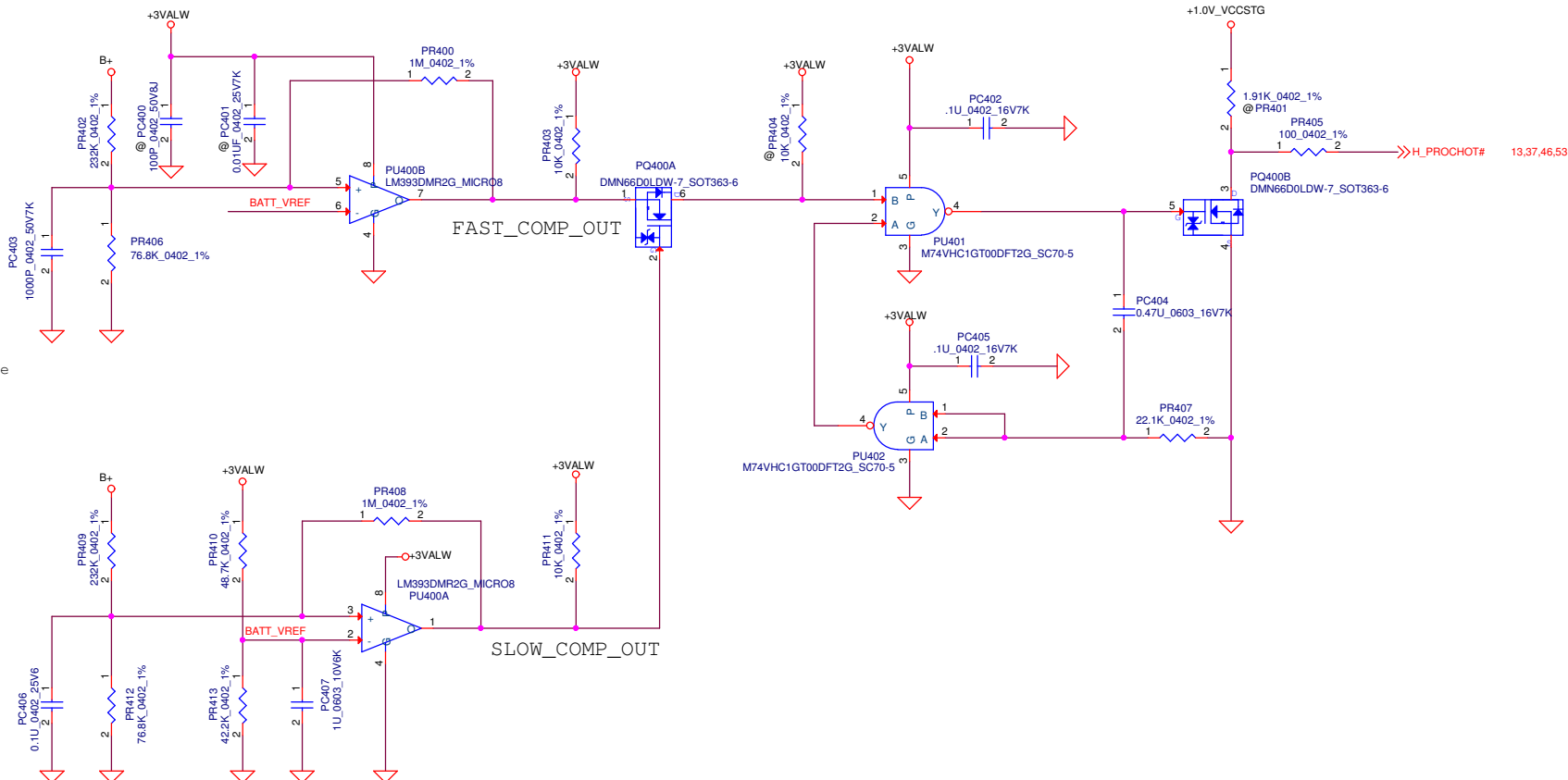


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PU400 Main source  
PQ400B open at 3/5V\_B+ below 5.73V  
and 3/5V\_B+ recover 6.05V PQ400B close



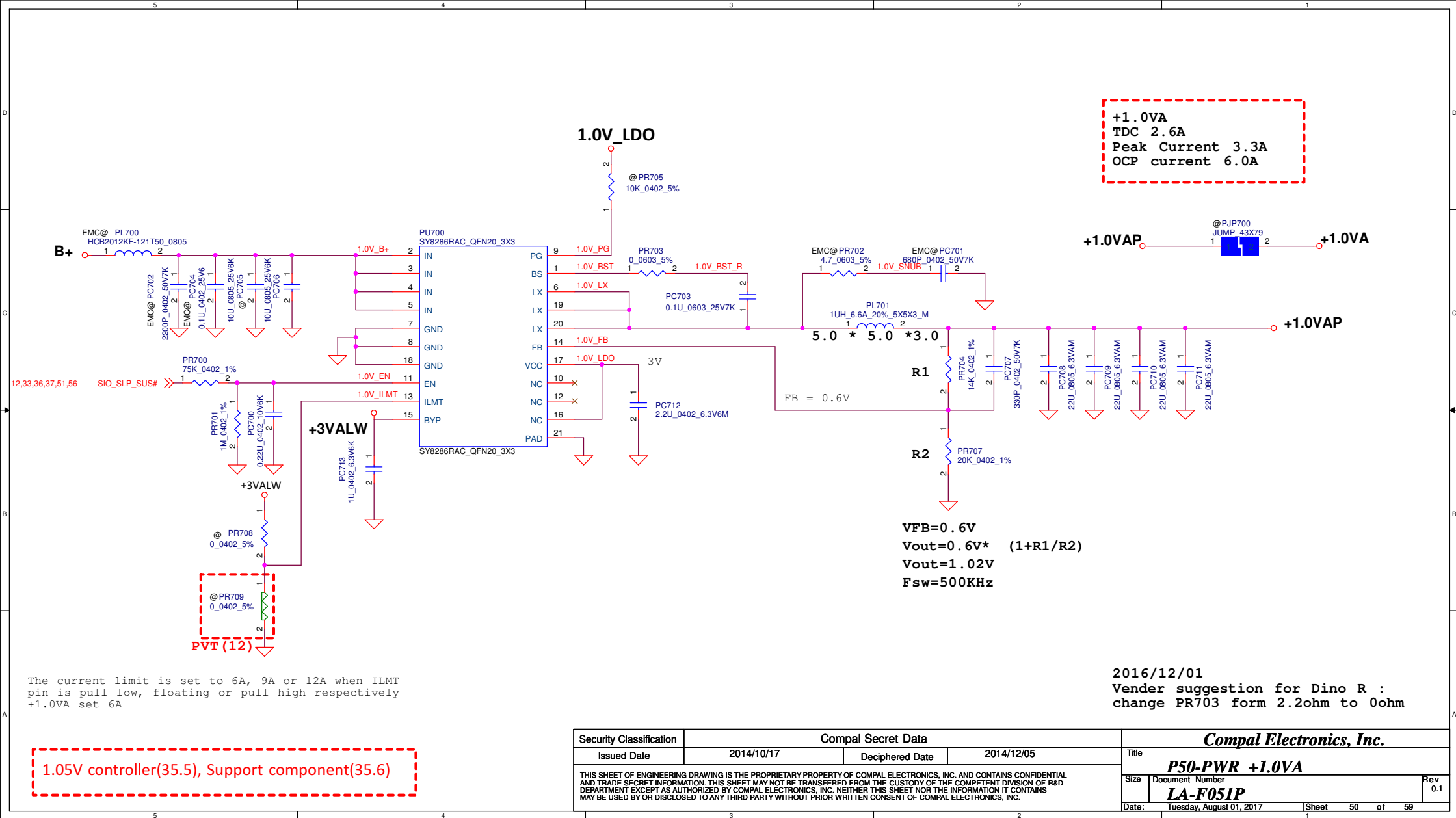
Component (37.1)

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					Date:	Tuesday, August 01, 2017	Sheet 47 of 59

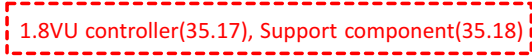






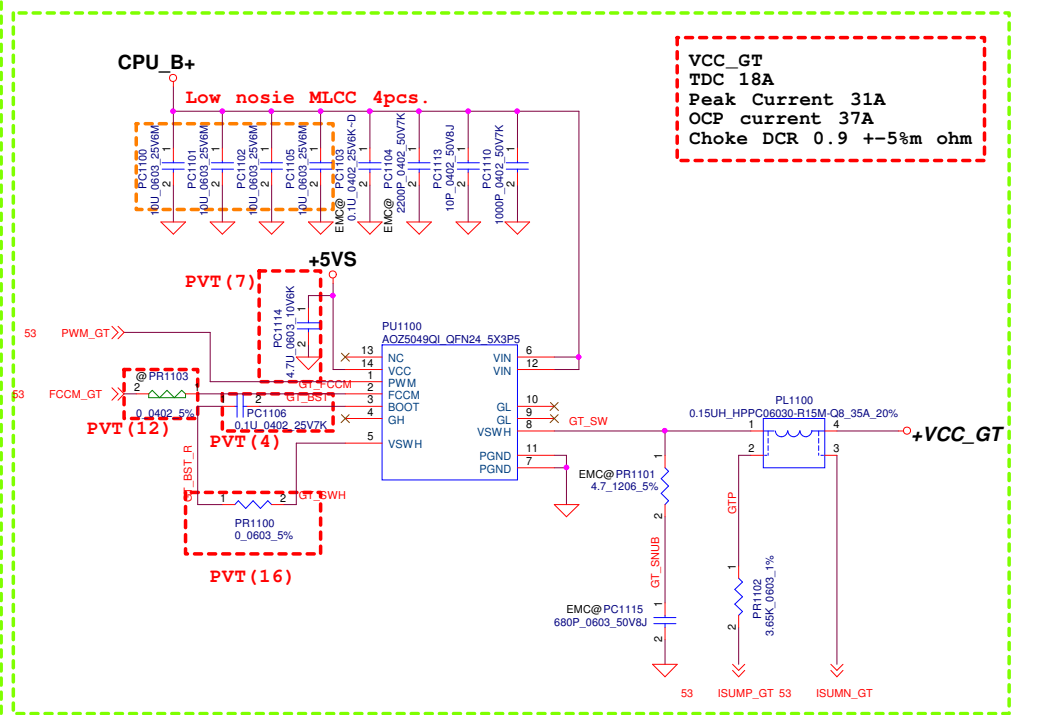
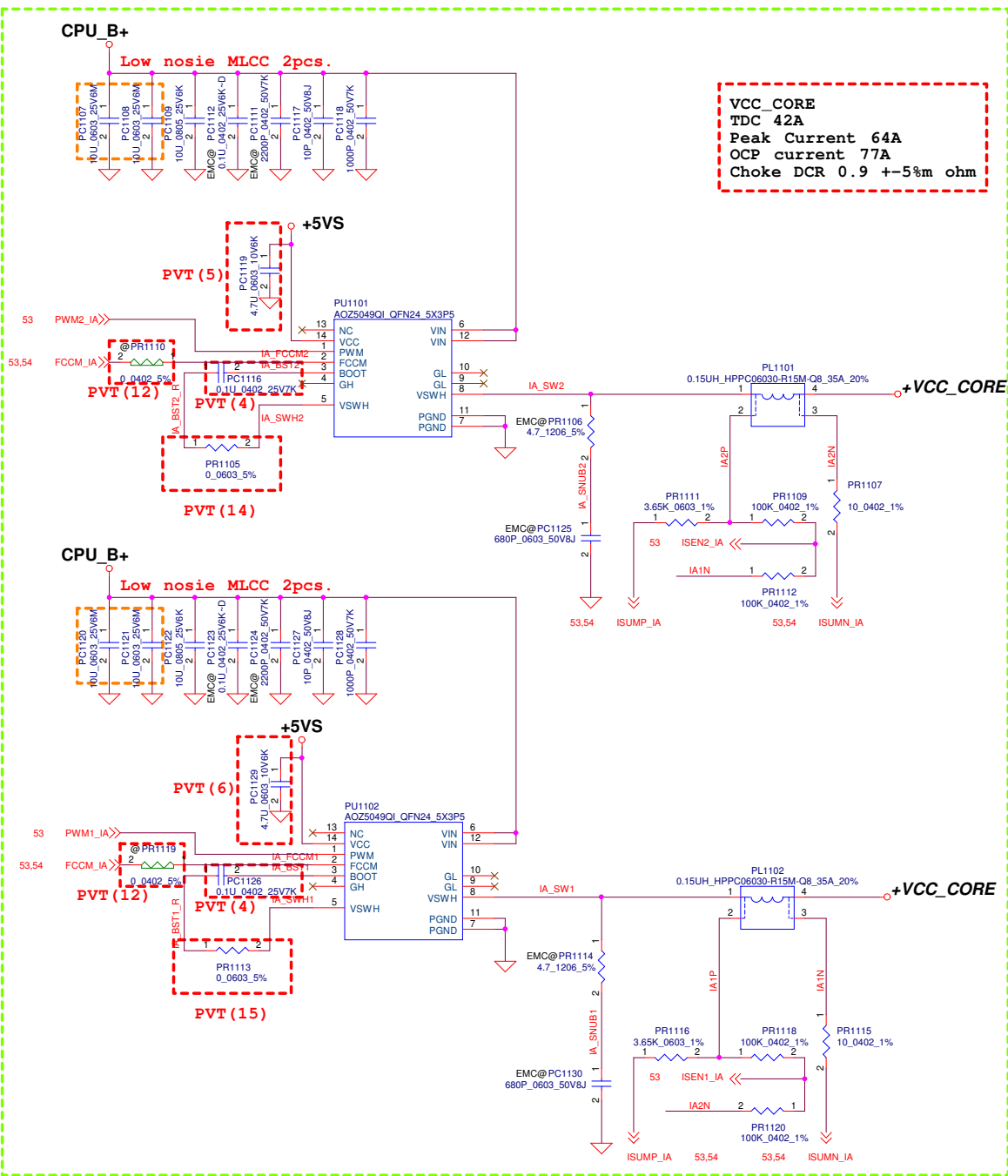






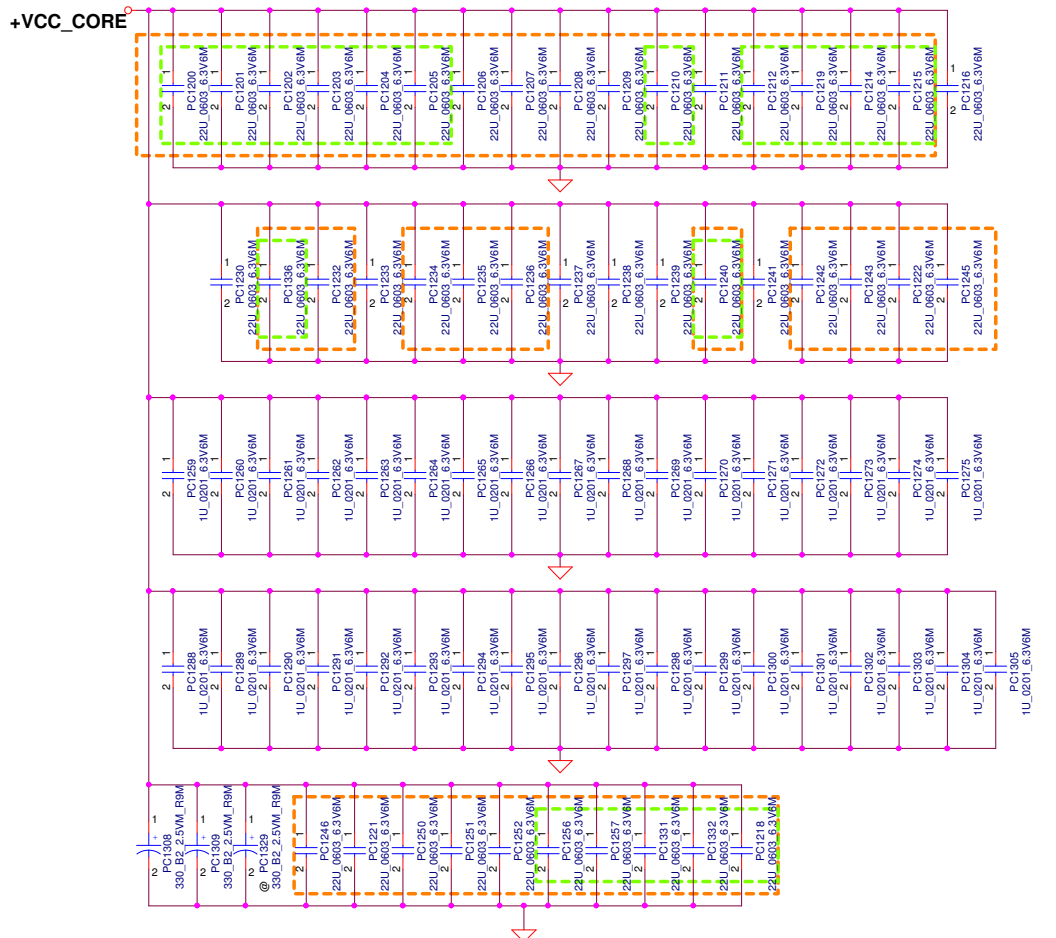
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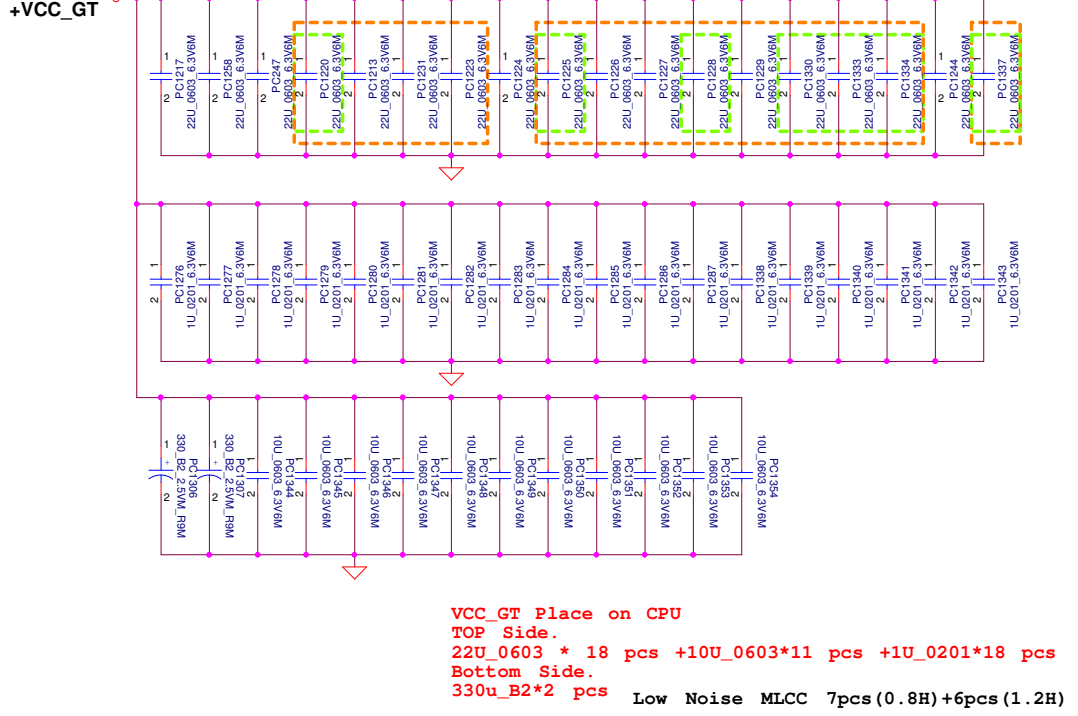
VCC\_CORE controller(36.1), Drivers (36.2), Support component(36.3)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	
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Size		Document Number		Rev	
LA-F051P		LA-F051P		0.1	
Date:		Tuesday, August 01, 2017		ISheet	
		54		of	
		59			

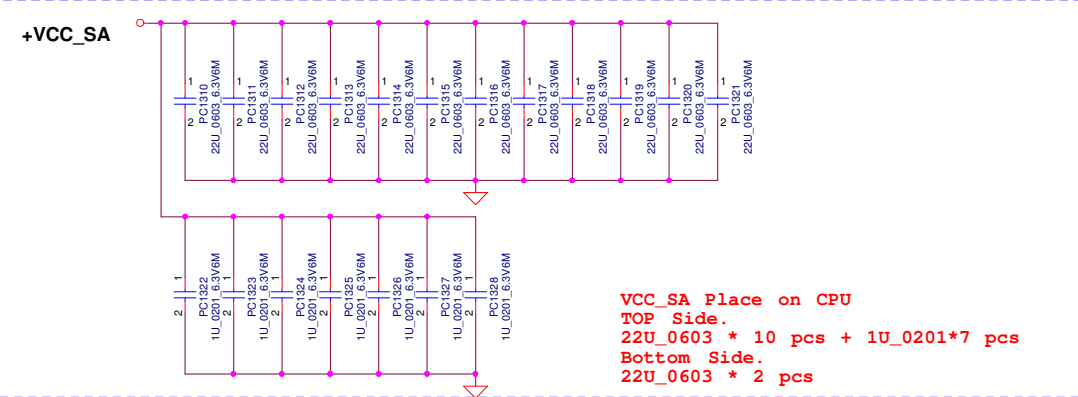


**VCC\_CORE Place on CPU**  
**TOP Side.**  
 22U\_0603 \* 36 pcs +1U\_0201\*33 pcs  
**Bottom Side.**  
 330u\_B2\*3 pcs + 22U\_0603 \* 7 pcs + 1U\_0201 \*2      Low Noise MLCC 18pcs(0.8H)+18pcs(1.2H)

VCC\_CORE output cap(36.4), VCC\_GT output cap(36.5), VCC\_SA output cap(36.6)



**VCC\_GT Place on CPU**  
**TOP Side.**  
 22U\_0603 \* 18 pcs +10U\_0603\*11 pcs +1U\_0201\*18 pcs  
**Bottom Side.**  
 330u\_B2\*2 pcs      Low Noise MLCC 7pcs(0.8H)+6pcs(1.2H)



**VCC\_SA Place on CPU**  
**TOP Side.**  
 22U\_0603 \* 10 pcs + 1U\_0201\*7 pcs  
**Bottom Side.**  
 22U\_0603 \* 2 pcs

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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	P55-PWR CPU BACK SIDE MLCC
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[AC in]				[Battery only, AC absent]			
ITEM	Measure Point		Time	ITEM	Measure Point		Time
Ta	-DC_IN	To	+3V_Vc	Ta	ALWON	To	+3VALW
Tb	-DC_IN	To	ACAV_IN	Tb	ALWON	To	+3VALW
Tc	-DC_IN	To	B+	Tc	ALWON	To	+3VALW
Td	ACAV_IN	To	ALWON	Td	ALWON	To	+3VALW
Te	ALWON	To	+3VALW	Te	ALWON	To	+3VALW
Tf	ALWON	To	+3VALW	Tf	ALWON	To	+3VALW
Tg	+3VALW	To	ALW_PWRSD 3V 5V	Tg	+3VALW	To	ALW_PWRSD 3V 5V
Th	ALWON	To	PCH_DPWRDR	Th	ALWON	To	PCH_DPWRDR
Ti	B+	To	+3VLP	Ti	B+	To	+3VLP
Tj	POWER_SW_IN#	To	POWER_SW_IN#	Tj	POWER_SW_IN#	To	POWER_SW_IN#
				Tk	ALWON	To	+3V_Vc
				Ym	B+	To	+3V_Vc

ITEM	Measure Point	Time
11	+3VALW	to SIO_SLP_SUS#
12	SIO_SLP_SUS#	to /M_PCH
13	SIO_SLP_SUS#	to /M_VA
14	SIO_SLP_SUS#	to /10V_PRM_CORE
15	SIO_SLP_SUS#	to /10VA
16	+3VALW	to MPPHY_PWR_EN
17	MPPHY_PWR_EN	to /10V_MPHYGT
18	SIO_SLP_SUS#	to SUBCKE
19	+10VA	to PCH_RSMRST#
20	PCH_RSMRST#	to AC_PRESENT
21	PCH_RSMRST#	to SIO_SLP_S#
22	SIO_SLP_S#	to SIO_SLP_W#
23	SIO_SLP_S#	to SIO_SLP_WLAN#
24	SIO_SLP_WLAN#	to AUX_EN_WOVL
25	AUX_EN_WOVL	to /3VS_NGPF
26	SIO_SLP_S#	to SIO_SLP_S#
27	SIO_SLP_S#	to /3VS_VCGST
28	SIO_SLP_S#	to BUS_ON_EC
29	SUS_ON_EC	to /18VU
30	SUS_ON_EC	to /12V_DDR
31	SIO_SLP_S#	to /SIO_PWRRO
32	SIO_SLP_S#	to SIO_SLP_S#
33	SIO_SLP_S#	to RUN_ON_EC
34	RUN_ON_EC	to /33V0V_SSD
35	RUN_ON_EC	to /10VS_VCGST
36	RUN_ON_EC	to /10VS_VCGD
37	RUN_ON_EC	to /3VS
38	RUN_ON_EC	to /5VS
39	+3VS	to RUNPWROK
40	+3VS	to MPP_VR_ON
41	MPP_VR_ON	to CORE_PG (PCH_PWROK)
42	VCCORE_PG (PCH_PWROK)	to VCC_SA
43	MPP_VR_ON	to VCC_EDRAM
44	MPP_VR_ON	to VCC_EOPD
45	MPP_VR_ON	to SYS_PWRON (RESET_OUT#)
46	PCH_PUSTR#	to VCC_CORE
47	PCH_PUSTR#	to VCC_GDT